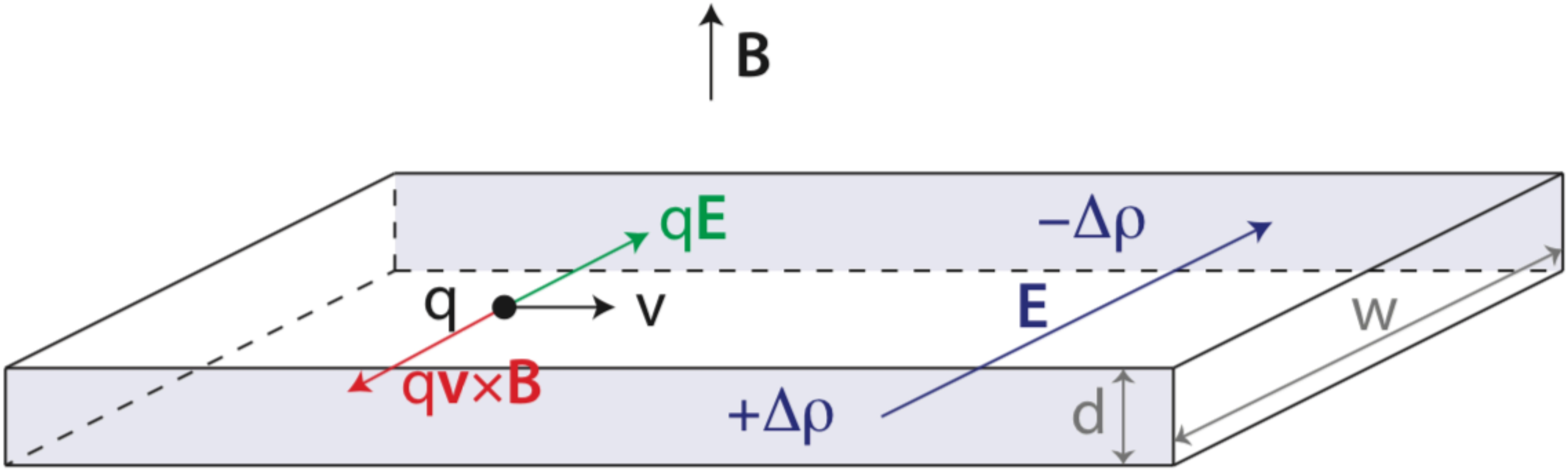
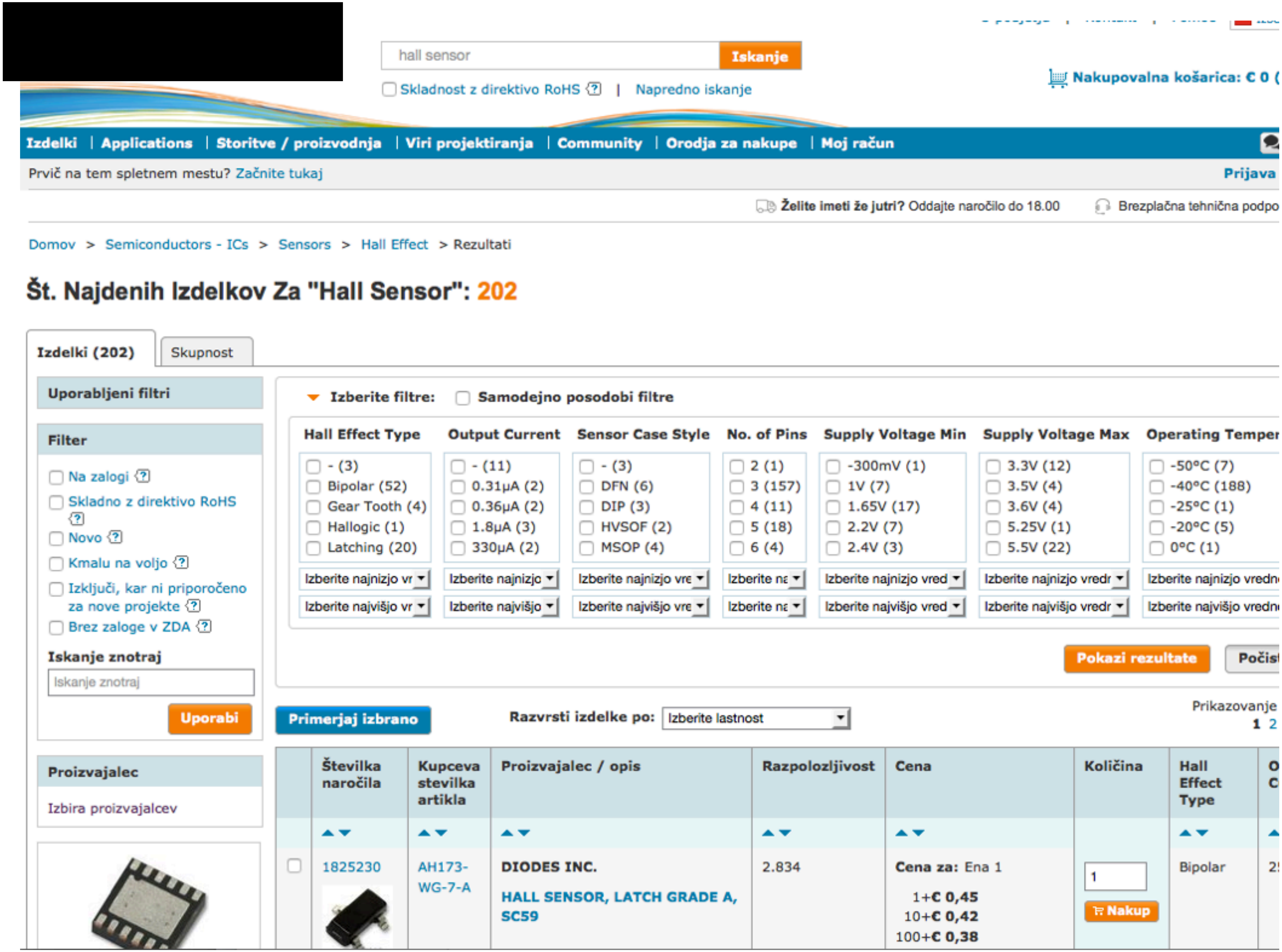
POLPREVODNIŠKE NAPRAVE

Hallov pojav



$qvB = qE, \quad \text{torej} \quad vB = E$ $\qquad j = qvn$

Hallov koeficient: $R_H = \dfrac{E}{jB} = \dfrac{1}{qn}$



[redacted]

hall sensor **Iskanje**

☐ Skladnost z direktivo RoHS | Napredno iskanje

Nakupovalna košarica: € 0 (

Izdelki | **Applications** | **Storitve / proizvodnja** | **Viri projektiranja** | **Community** | **Orodja za nakupe** | **Moj račun**

Prvič na tem spletnem mestu? Začnite tukaj **Prijava**

Želite imeti že jutri? Oddajte naročilo do 18.00 Brezplačna tehnična podpo

Domov > Semiconductors - ICs > Sensors > Hall Effect > Rezultati

Št. Najdenih Izdelkov Za "Hall Sensor": 202

Izdelki (202) Skupnost

Uporabljeni filtri

Filter

- ☐ Na zalogi
- ☐ Skladno z direktivo RoHS
- ☐ Novo
- ☐ Kmalu na voljo
- ☐ Izključi, kar ni priporočeno za nove projekte
- ☐ Brez zaloge v ZDA

Iskanje znotraj

Iskanje znotraj

Uporabi

Proizvajalec

Izbira proizvajalcev

Izberite filtre: ☐ **Samodejno posodobi filtre**

Hall Effect Type	Output Current	Sensor Case Style	No. of Pins	Supply Voltage Min	Supply Voltage Max	Operating Temper
☐ - (3)	☐ - (11)	☐ - (3)	☐ 2 (1)	☐ -300mV (1)	☐ 3.3V (12)	☐ -50°C (7)
☐ Bipolar (52)	☐ 0.31µA (2)	☐ DFN (6)	☐ 3 (157)	☐ 1V (7)	☐ 3.5V (4)	☐ -40°C (188)
☐ Gear Tooth (4)	☐ 0.36µA (2)	☐ DIP (3)	☐ 4 (11)	☐ 1.65V (17)	☐ 3.6V (4)	☐ -25°C (1)
☐ Hallogic (1)	☐ 1.8µA (3)	☐ HVSOF (2)	☐ 5 (18)	☐ 2.2V (7)	☐ 5.25V (1)	☐ -20°C (5)
☐ Latching (20)	☐ 330µA (2)	☐ MSOP (4)	☐ 6 (4)	☐ 2.4V (3)	☐ 5.5V (22)	☐ 0°C (1)
Izberite najnizjo vr	Izberite najnizjo	Izberite najnizjo vre	Izberite na	Izberite najnizjo vred	Izberite najnizjo vredr	Izberite najnizjo vredn
Izberite najvišjo vr	Izberite najvišjo	Izberite najvišjo vre	Izberite na	Izberite najvišjo vred	Izberite najvišjo vredr	Izberite najvišjo vredn

Pokazi rezultate **Počis**

Primerjaj izbrano **Razvrsti izdelke po:** Izberite lastnost

Prikazovanje **1** 2

	Številka naročila	Kupceva stevilka artikla	Proizvajalec / opis	Razpolozljivost	Cena	Količina	Hall Effect Type	O C
☐	1825230	AH173-WG-7-A	**DIODES INC.** **HALL SENSOR, LATCH GRADE A, SC59**	2.834	**Cena za:** Ena 1 1+**€ 0,45** 10+**€ 0,42** 100+**€ 0,38**	1 **Nakup**	Bipolar	2

AH173

INTERNAL PULL-UP HALL EFFECT LATCH FOR HIGH TEMPERATURE

Description

AH173 is a single-digital-output Hall-Effect latch sensor with pull-up resistor for high temperature operation. The device includes an on-chip Hall voltage generator for magnetic sensing, an amplifier to amplify Hall voltage, a comparator to provide switching hysteresis for noise rejection, and an output driver with a pull-up resistor (Rpu). An internal band-gap regulator provides a temperature compensated supply voltage for internal circuits and allows a wide operating supply range.

When the magnetic flux density (**B**) is larger than operate point (**Bop**), output is switched on (OUT pin is pulled low). The output state is held on until a magnetic flux density reversal falls below Brp. When **B** is less than Brp, the output is switched off.

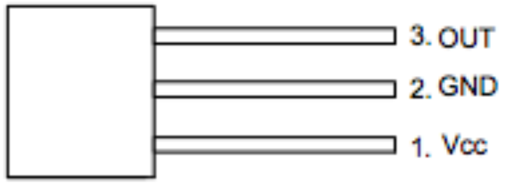
The AH173 is available in SIP-3L and SC59 packages.

Features

- Bipolar Hall-Effect latch sensor
- 3V to 20V DC operating voltage
- Built-in pull-up resistor
- 25mA output sink current
- Operating temperature: -40°C to +125°C
- SIP-3L and SC59 packages
  (SC59 is commonly known as SOT23 in Asia)
- Green Molding Compound (No Br, Sb) (Note 1)

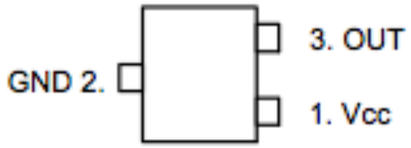
Pin Assignments

(Top View)



SIP-3L

(Top View)

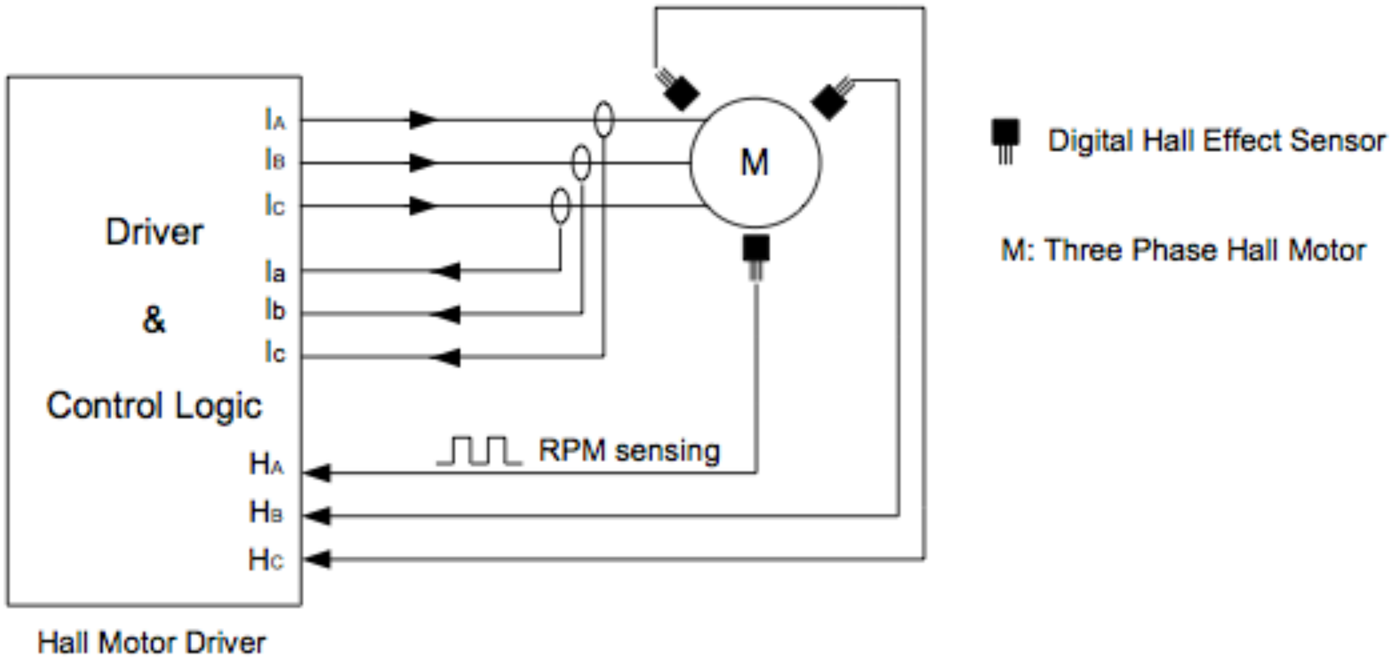


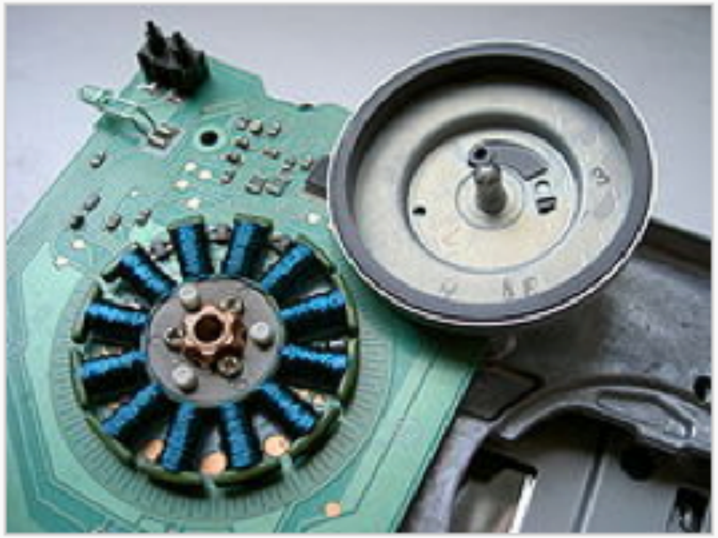
SC59

Applications

- Rotor Position Sensing
- Current Switch
- Encoder
- RPM Detection

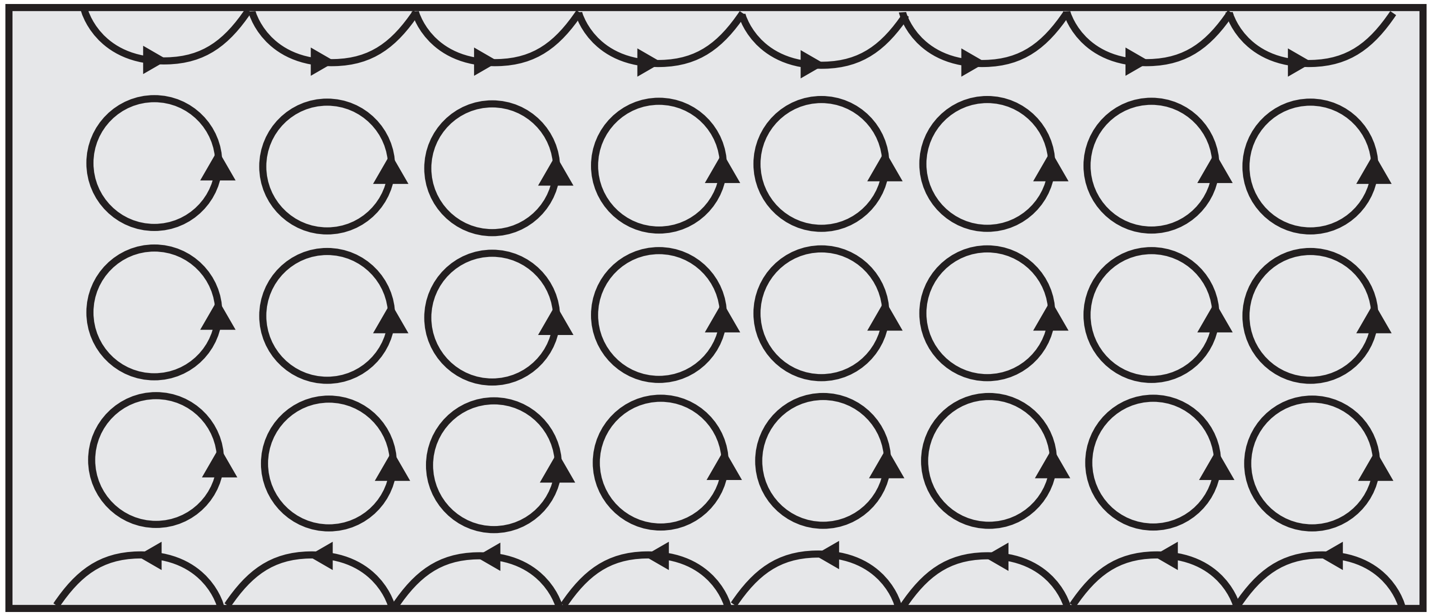
Typical Application Circuit



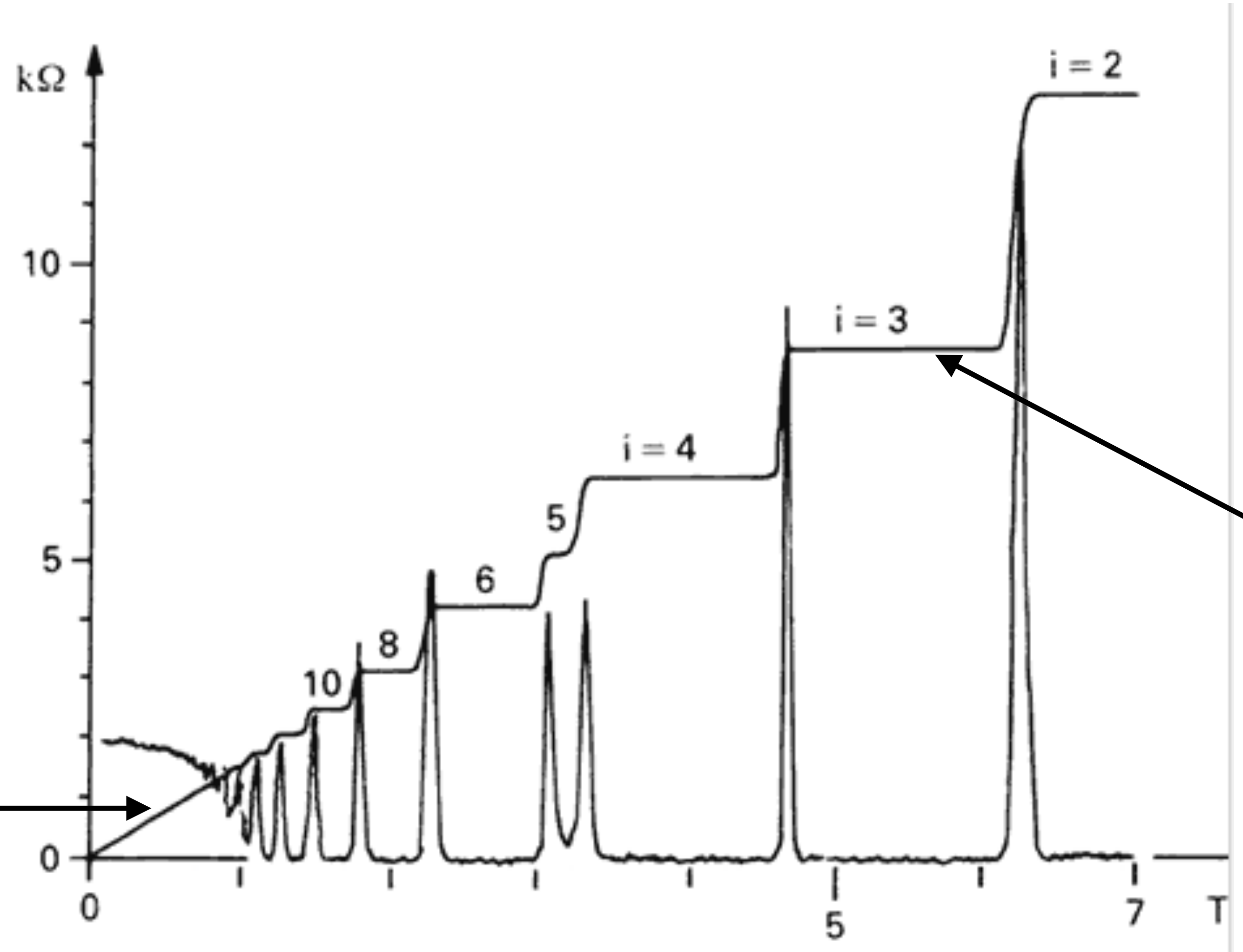


The motor from a 3.5" floppy disk drive. The coils, arranged radially, are made from copper wire coated with blue insulation. The rotor (upper right) has been removed and turned upside-down. The grey ring inside its cup is a permanent magnet.

Elektroni v močnem magnetnem polju



Integer quantum Hall effect (IQHE)



območje navadnega
Hallovega pojava

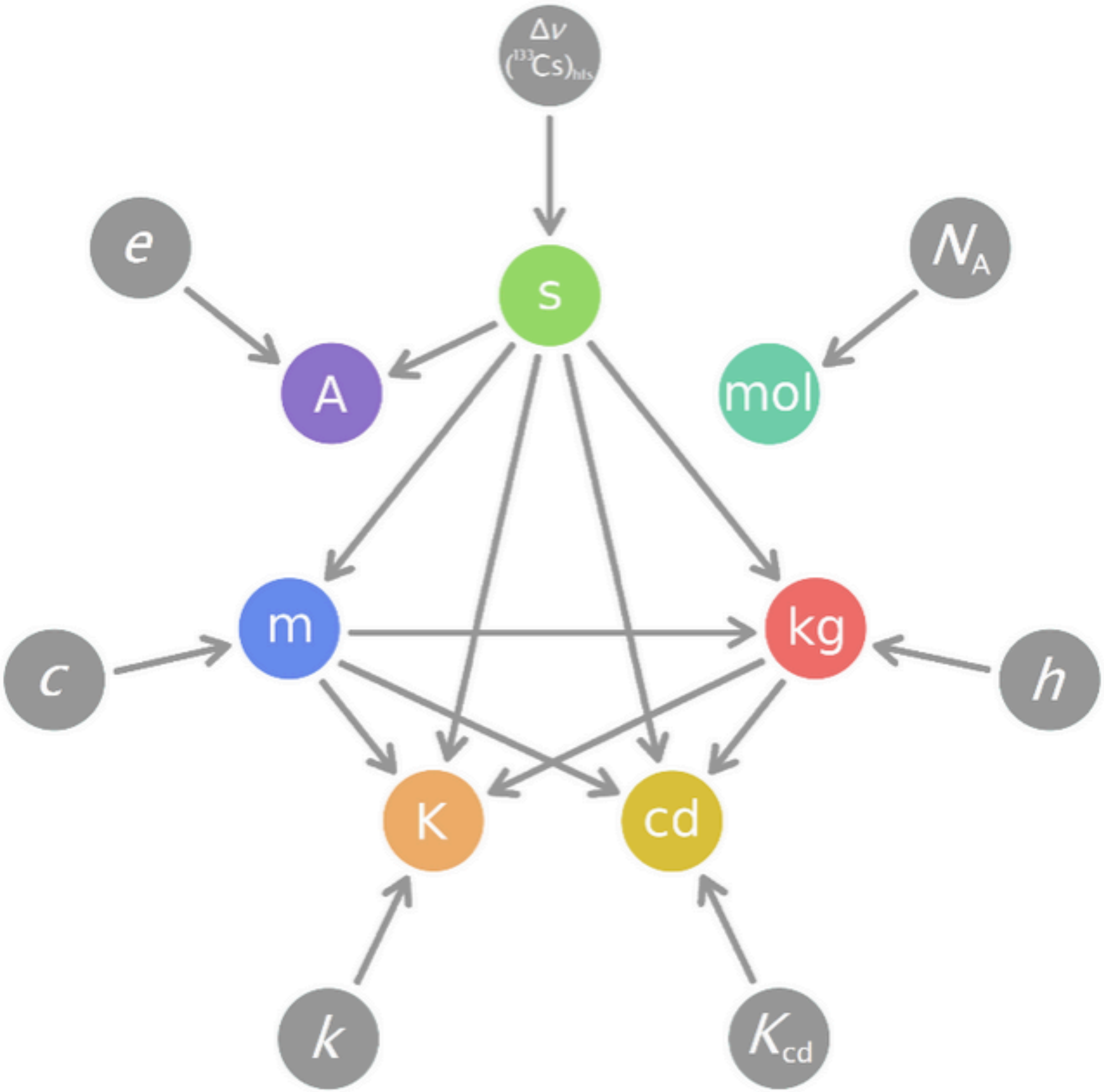
$$R = \frac{B}{qnd}$$

območje kvantnega
Hallovega pojava

$$R_K = \frac{h}{e^2} = 25812.807443\Omega \qquad R_H = R_K/N$$

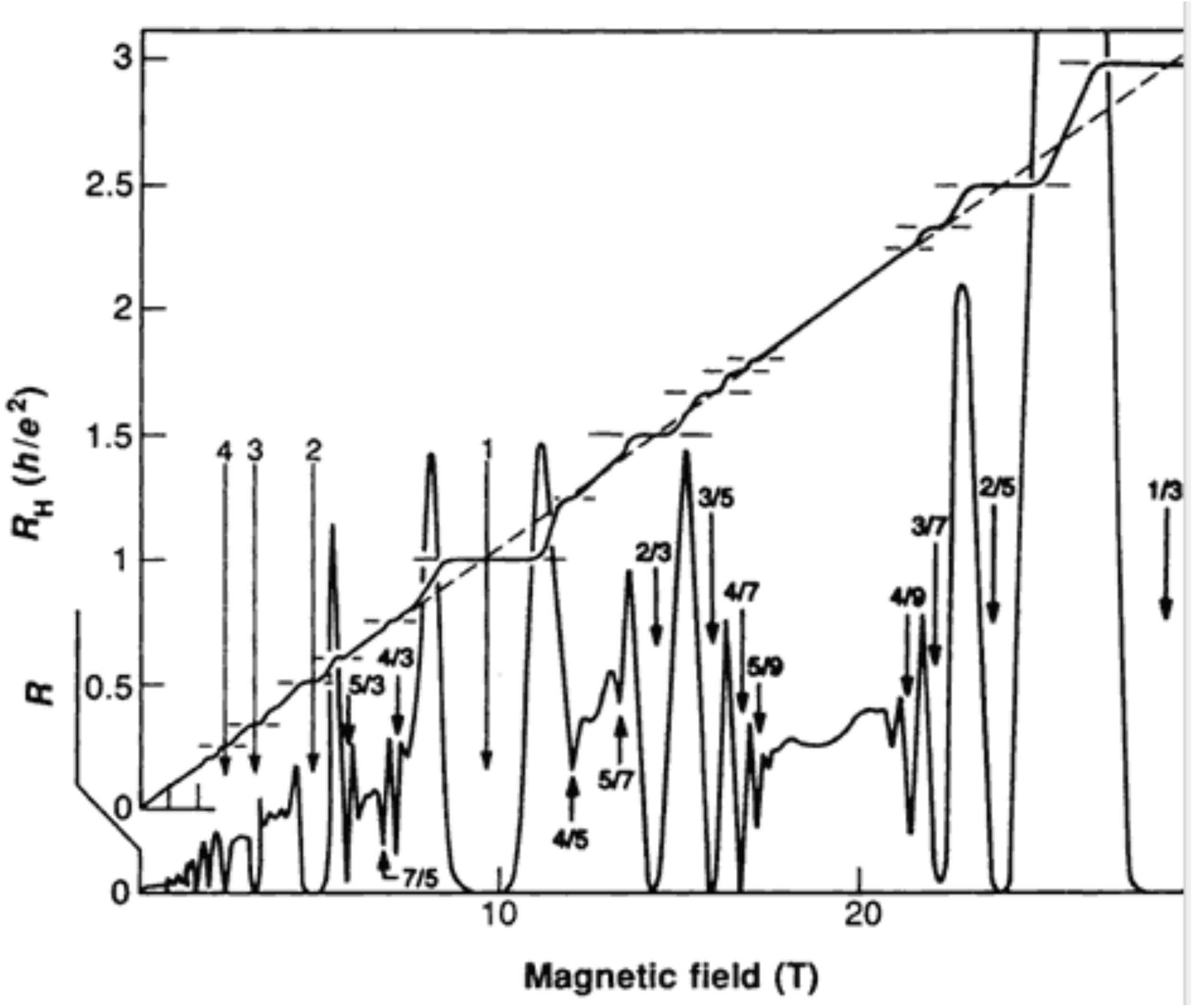
Nobelova: von Klitzing (1985)

Sprememba definicij enot SI (2019)



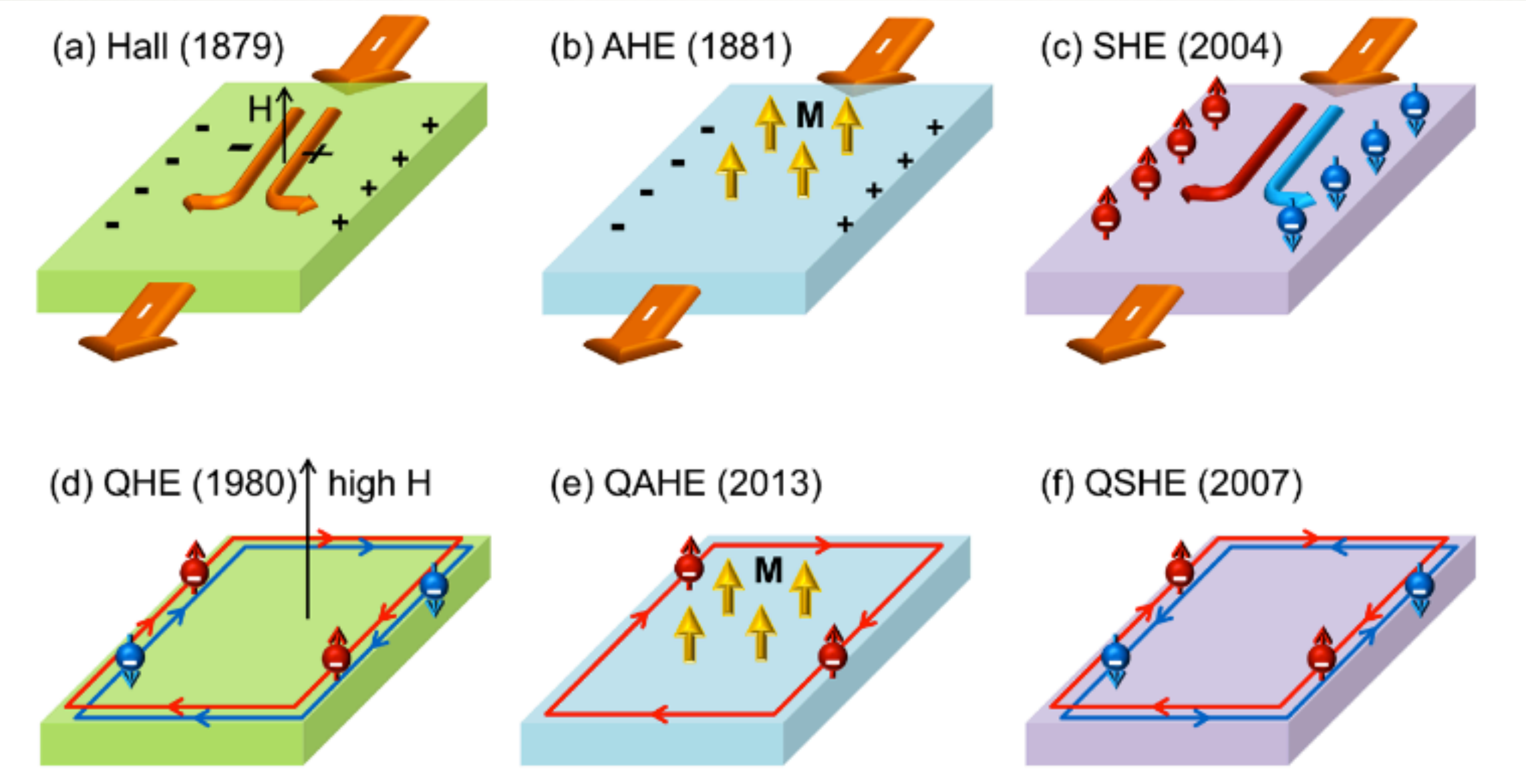
http://en.wikipedia.org/wiki/Proposed_redefinition_of_SI_base_units

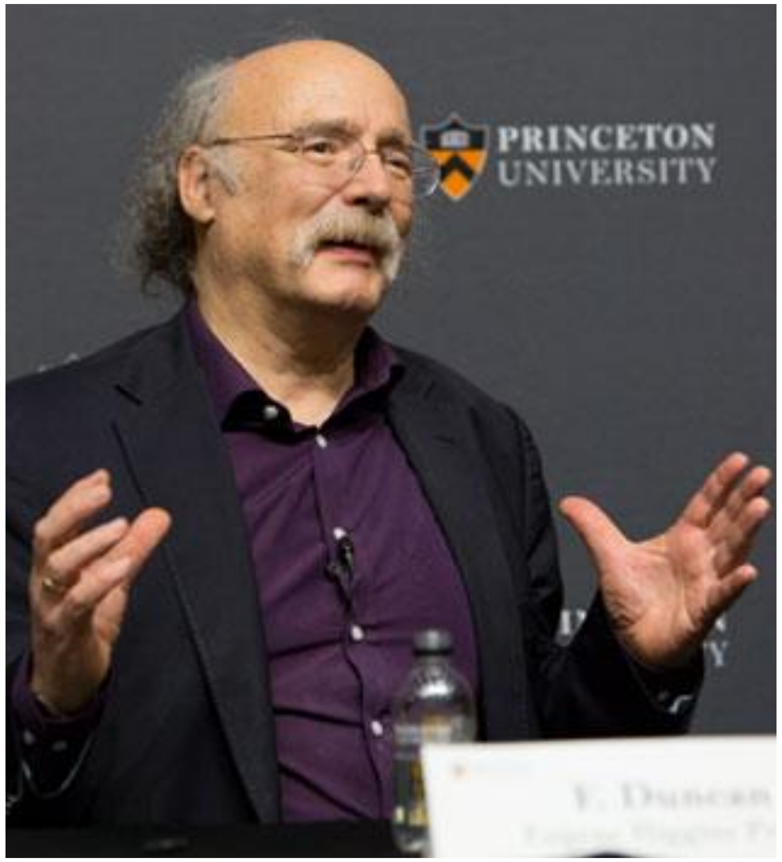
Fractional quantum Hall effect (FQHE)

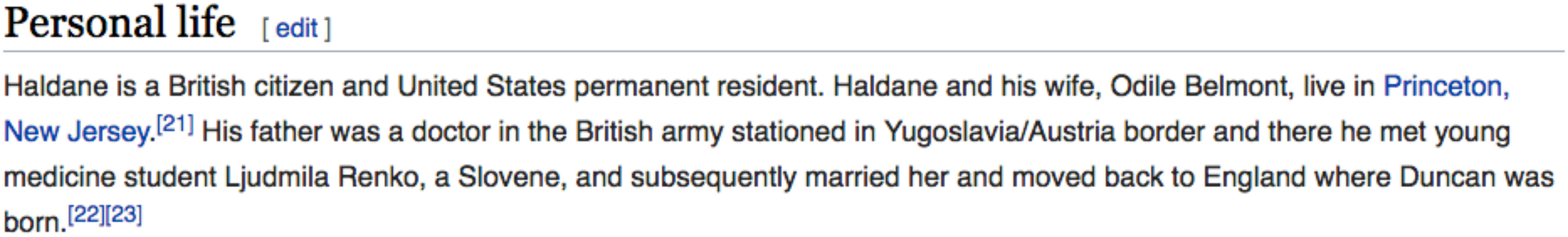


Nobelova: Laughlin, Stroemer, Tsui (1998)

Family of Hall effets

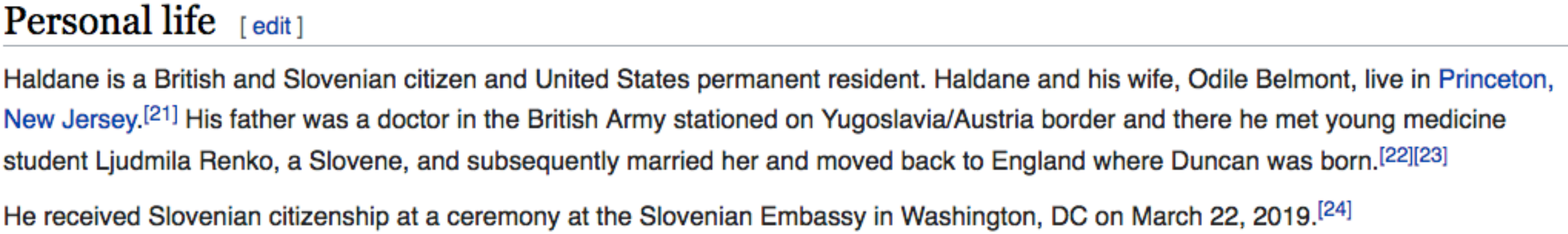






Personal life [edit]

Haldane is a British citizen and United States permanent resident. Haldane and his wife, Odile Belmont, live in Princeton, New Jersey.[21] His father was a doctor in the British army stationed in Yugoslavia/Austria border and there he met young medicine student Ljudmila Renko, a Slovene, and subsequently married her and moved back to England where Duncan was born.[22][23]



Personal life [edit]

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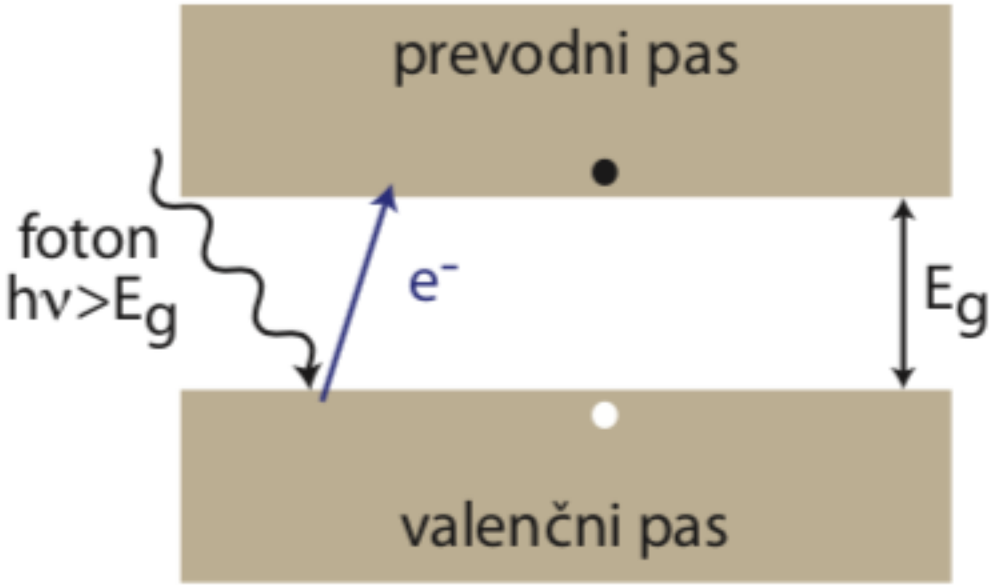
He received Slovenian citizenship at a ceremony at the Slovenian Embassy in Washington, DC on March 22, 2019.[24]

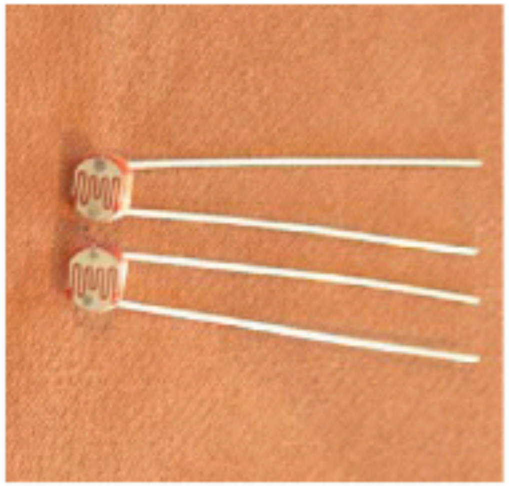
Nobelova: Kosterlitz, Haldane, Thouless (2016)

Fotoprevodnik



$$\sigma = qn\beta$$

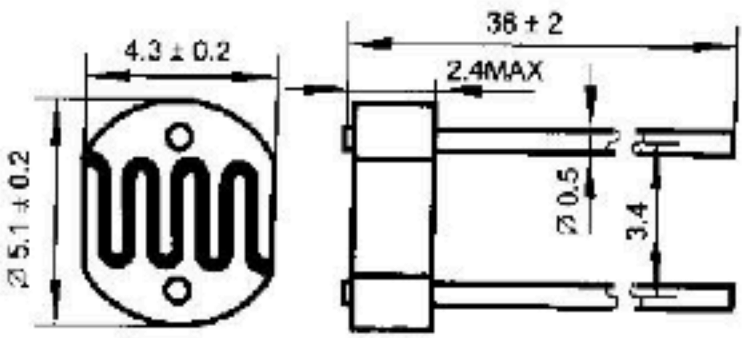
CdS PHOTOCONDUCTIVE CELLS GL5528



- Epoxy encapsulated
- Quick response
- Small size
- High sensitivity
- Reliable performance
- Good characteristic of spectrum

Light Resistance at 10Lux (at 25℃)	8~20KΩ
Dark Resistance at 0 Lux	1.0MΩ(min)
Gamma value at 100-10Lux	0.7
Power Dissipation(at 25℃)	100mW
Max Voltage (at 25℃)	150V
Spectral Response peak (at 25℃)	540nm
Ambient Temperature Range:	- 30~+70℃

Outline



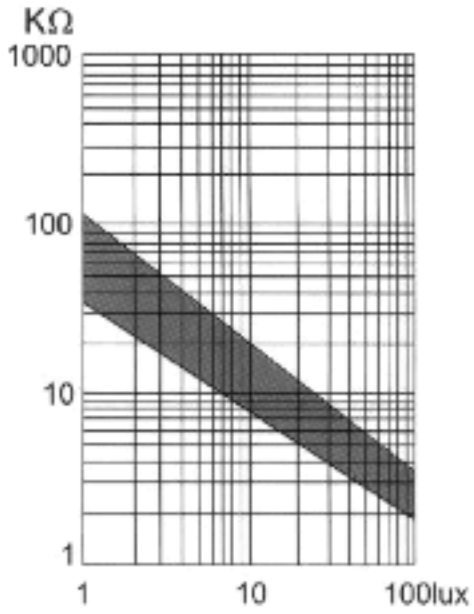
Measuring Conditions

1. Light Resistance:
   measured at 10 lux with standard light A (2854k color temperature) and 2h pre-illumination at 400-600 lux prior to testing.
2. Dark Resistance:
   measured 10 seconds after pulsed 10 lux.
3. Gamma Characteristic:
   between 10 lux and 100 lux and given by

   $$T = \frac{\log (R10/R100)}{\log (100/10)} = \log (R10/R100)$$

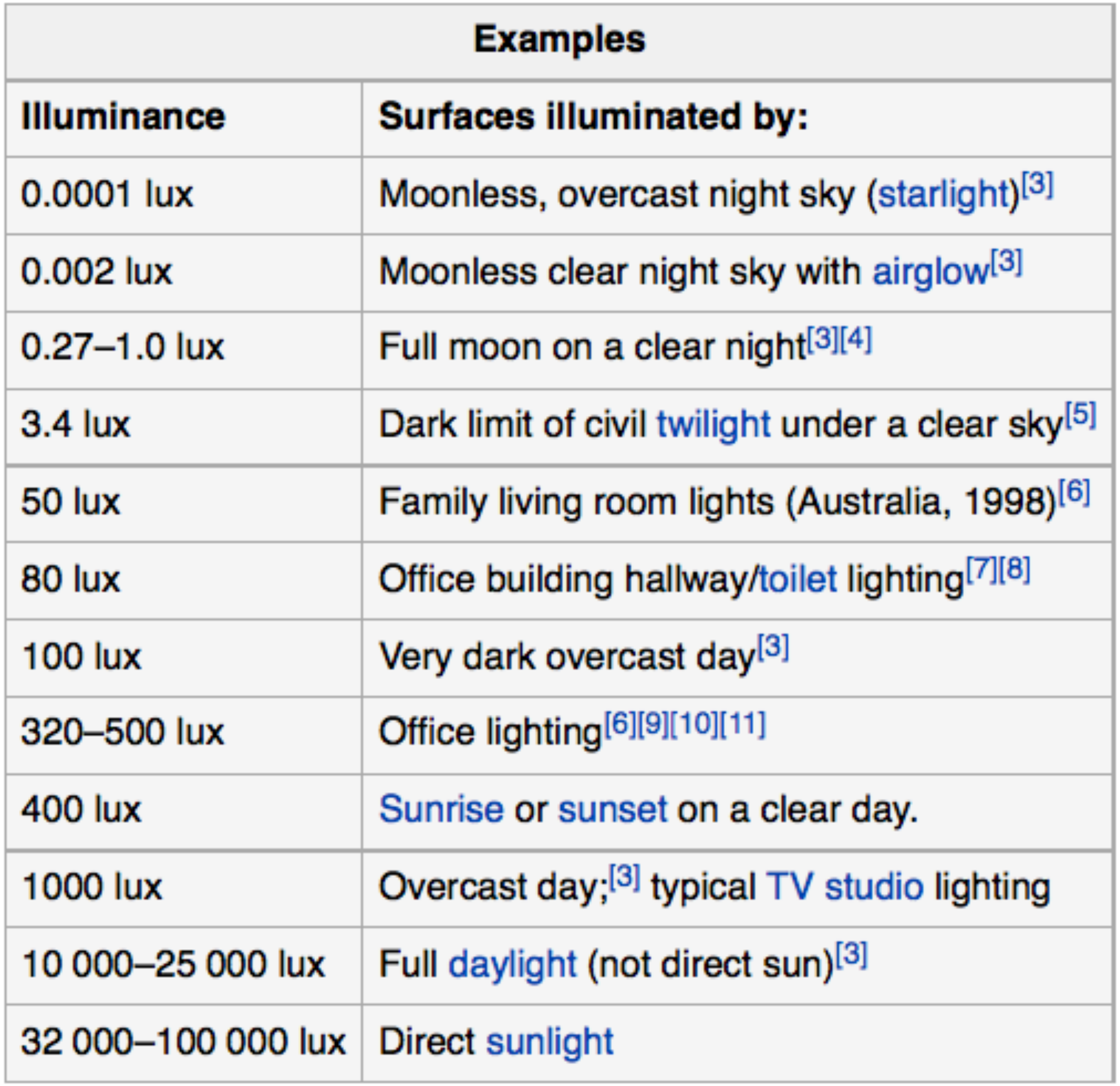
   R10, R100 cell resistance at 10 lux and 100 lux.
   The error of T is +0.1.
4. Pmax:
   Max. power dissipation at ambient temperature of 25°C.

Illuminance Vs. Photo Resistance



Osvetljenost

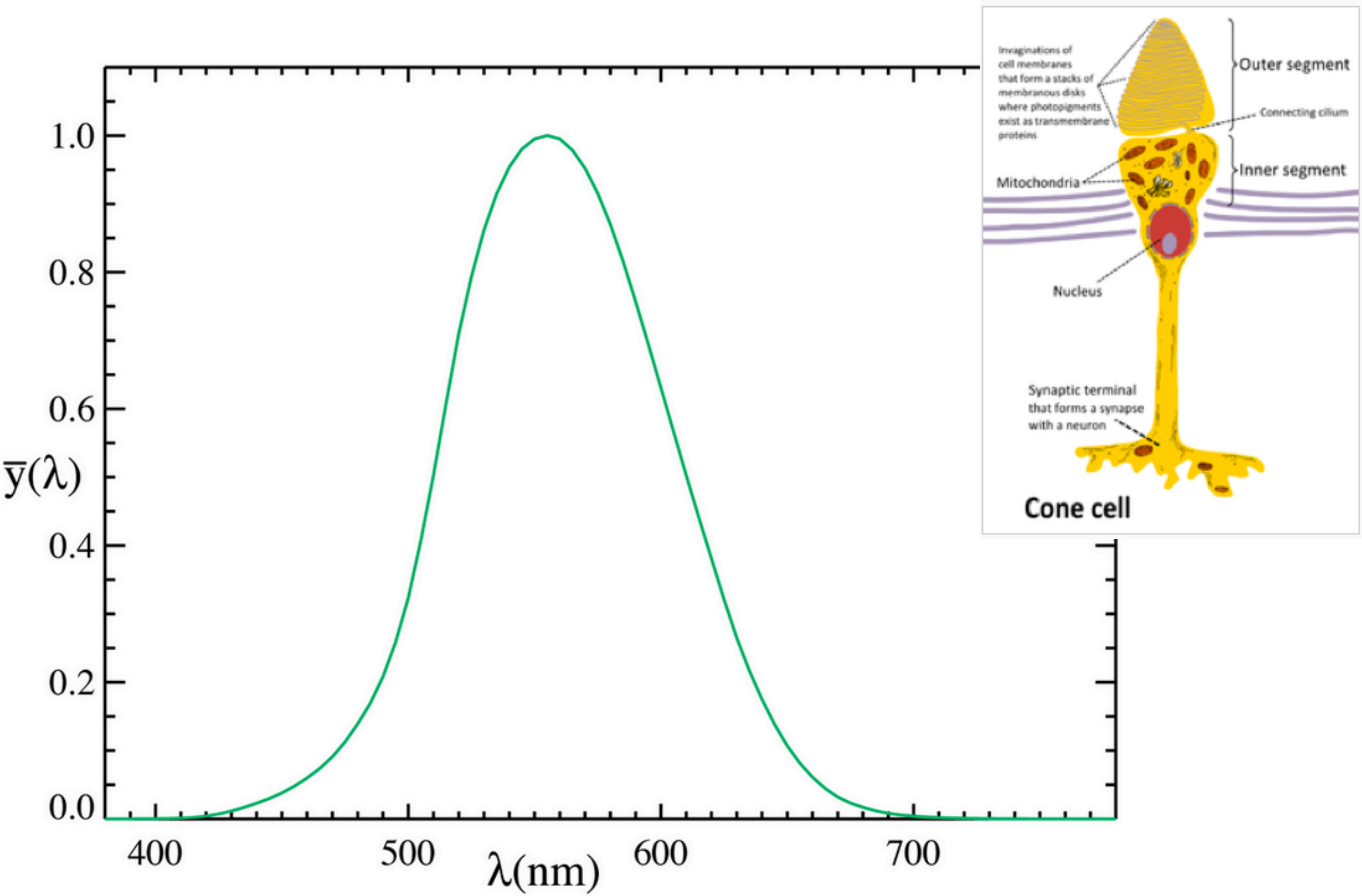
luks [lx] = lumen/kvadratni meter [lm/m^2]



Examples

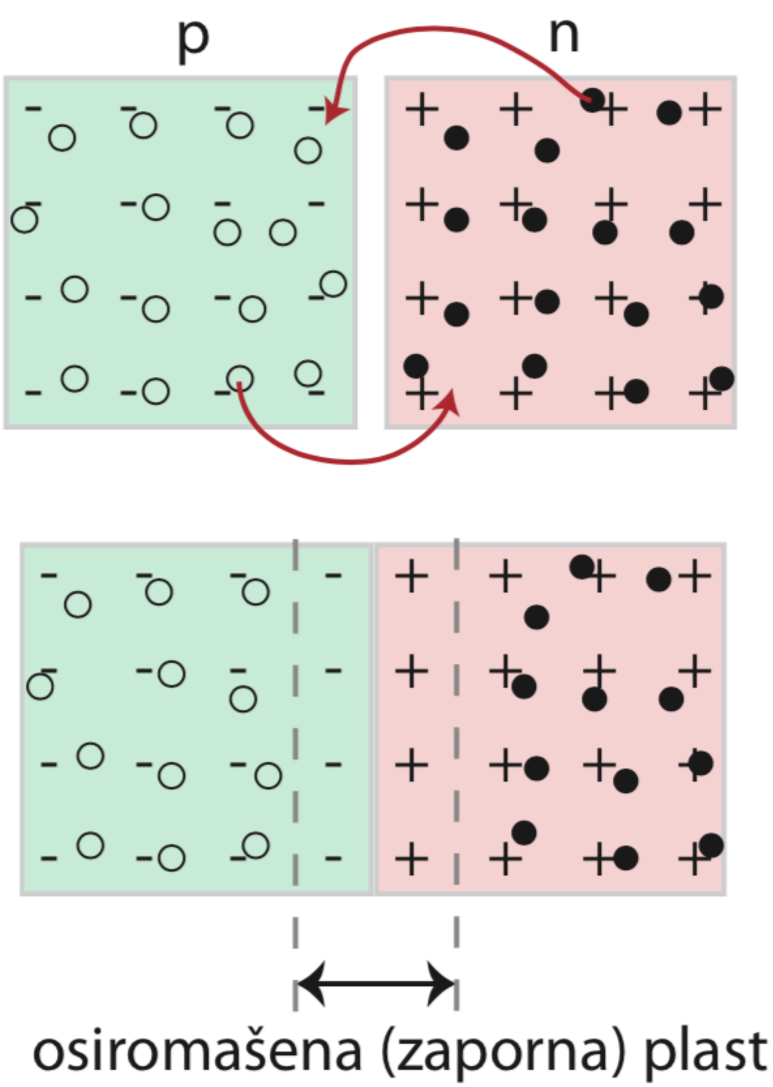
Illuminance	**Surfaces illuminated by:**
0.0001 lux	Moonless, overcast night sky (starlight)[3]
0.002 lux	Moonless clear night sky with airglow[3]
0.27–1.0 lux	Full moon on a clear night[3][4]
3.4 lux	Dark limit of civil twilight under a clear sky[5]
50 lux	Family living room lights (Australia, 1998)[6]
80 lux	Office building hallway/toilet lighting[7][8]
100 lux	Very dark overcast day[3]
320–500 lux	Office lighting[6][9][10][11]
400 lux	Sunrise or sunset on a clear day.
1000 lux	Overcast day;[3] typical TV studio lighting
10 000–25 000 lux	Full daylight (not direct sun)[3]
32 000–100 000 lux	Direct sunlight

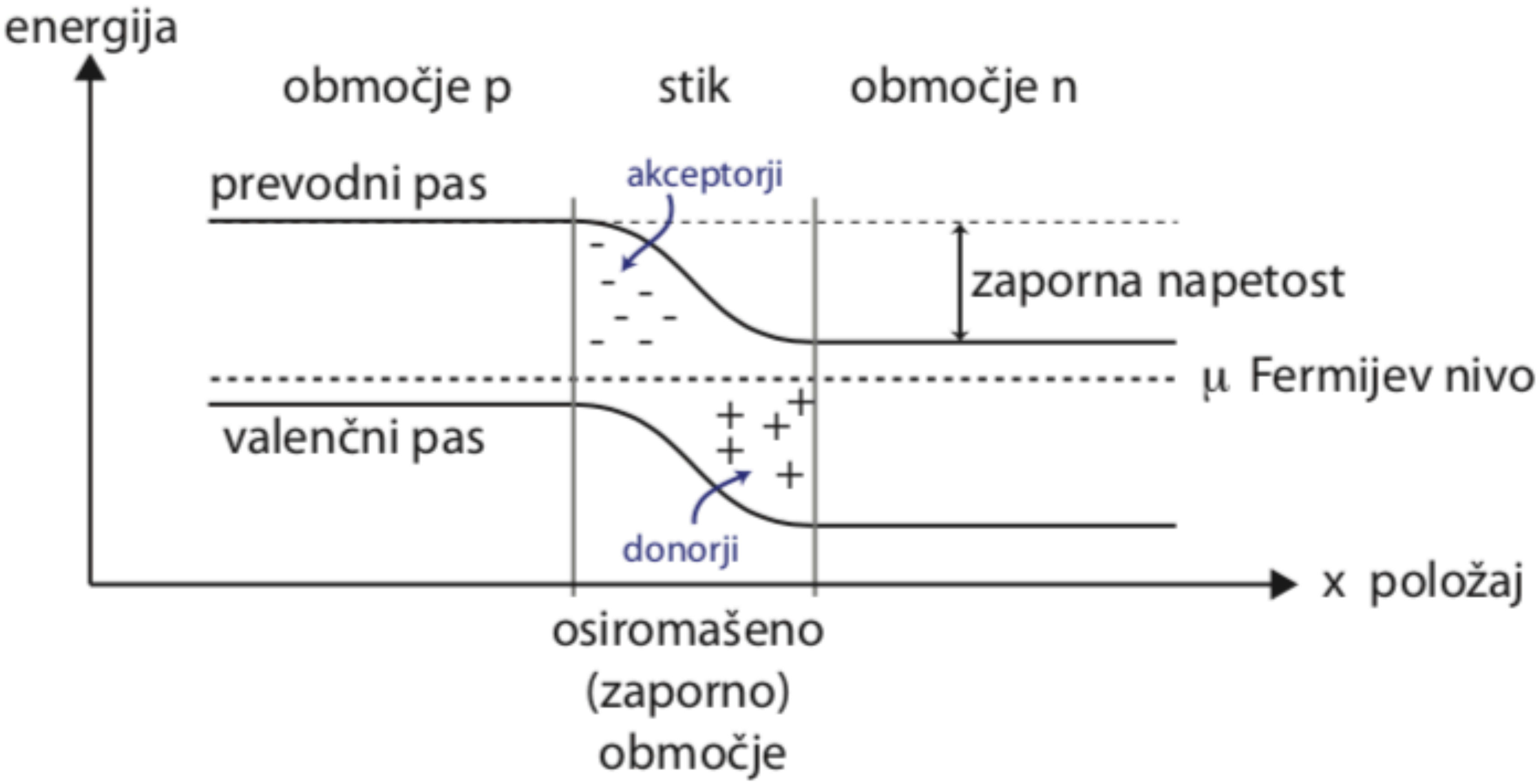
http://en.wikipedia.org/wiki/Lux

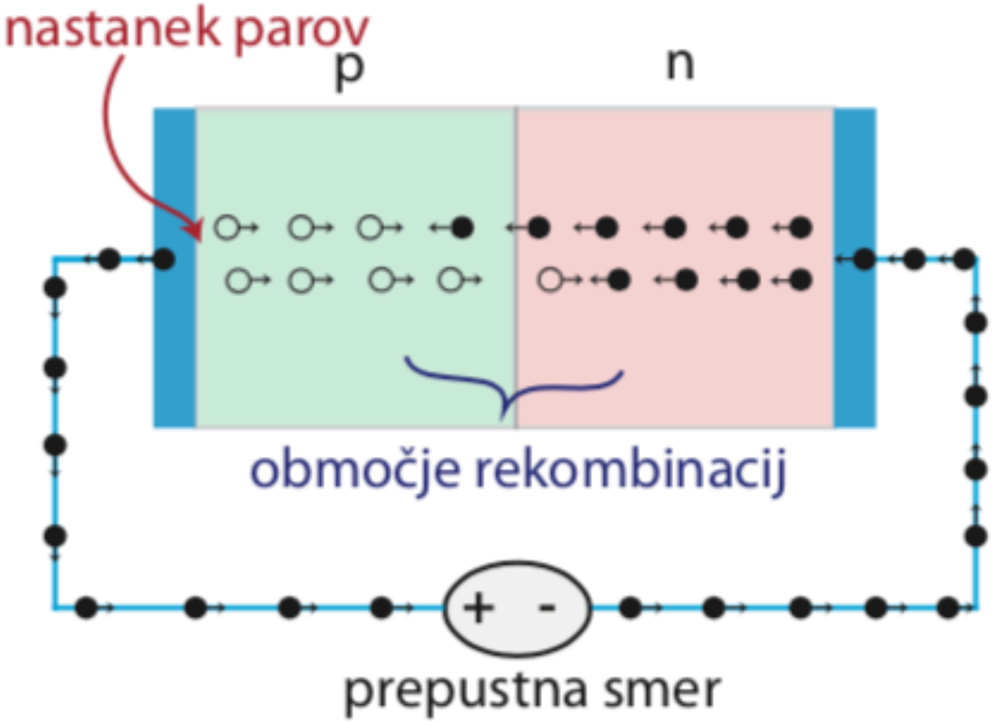


fotopična krivulja: največja občutljivost pri 550 nm

Dioda

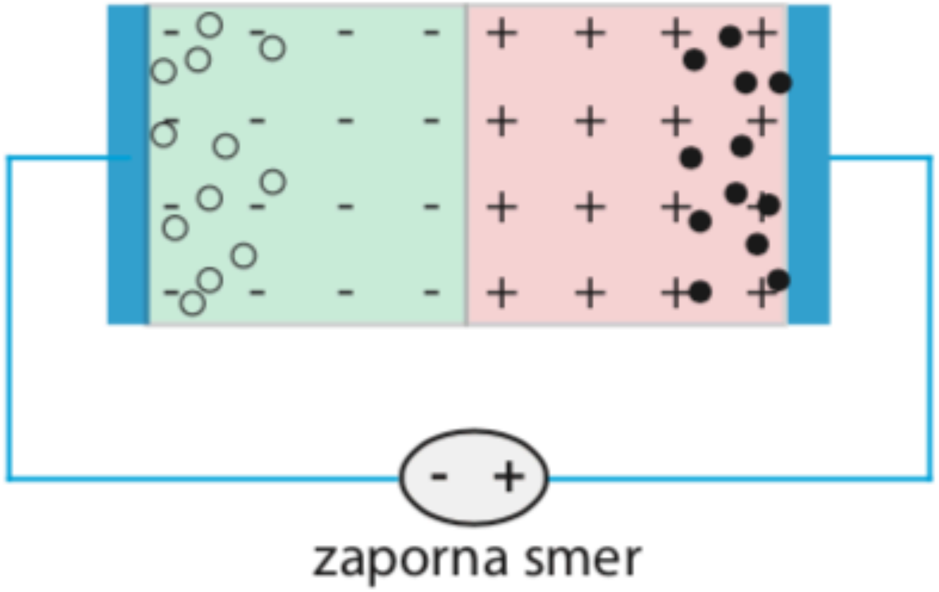

p
n
osiromašena (zaporna) plast


energija
območje p
stik
območje n
prevodni pas
akceptorji
zaporna napetost
µ Fermijev nivo
valenčni pas
donorji
x položaj
osiromašeno
(zaporno)
območje

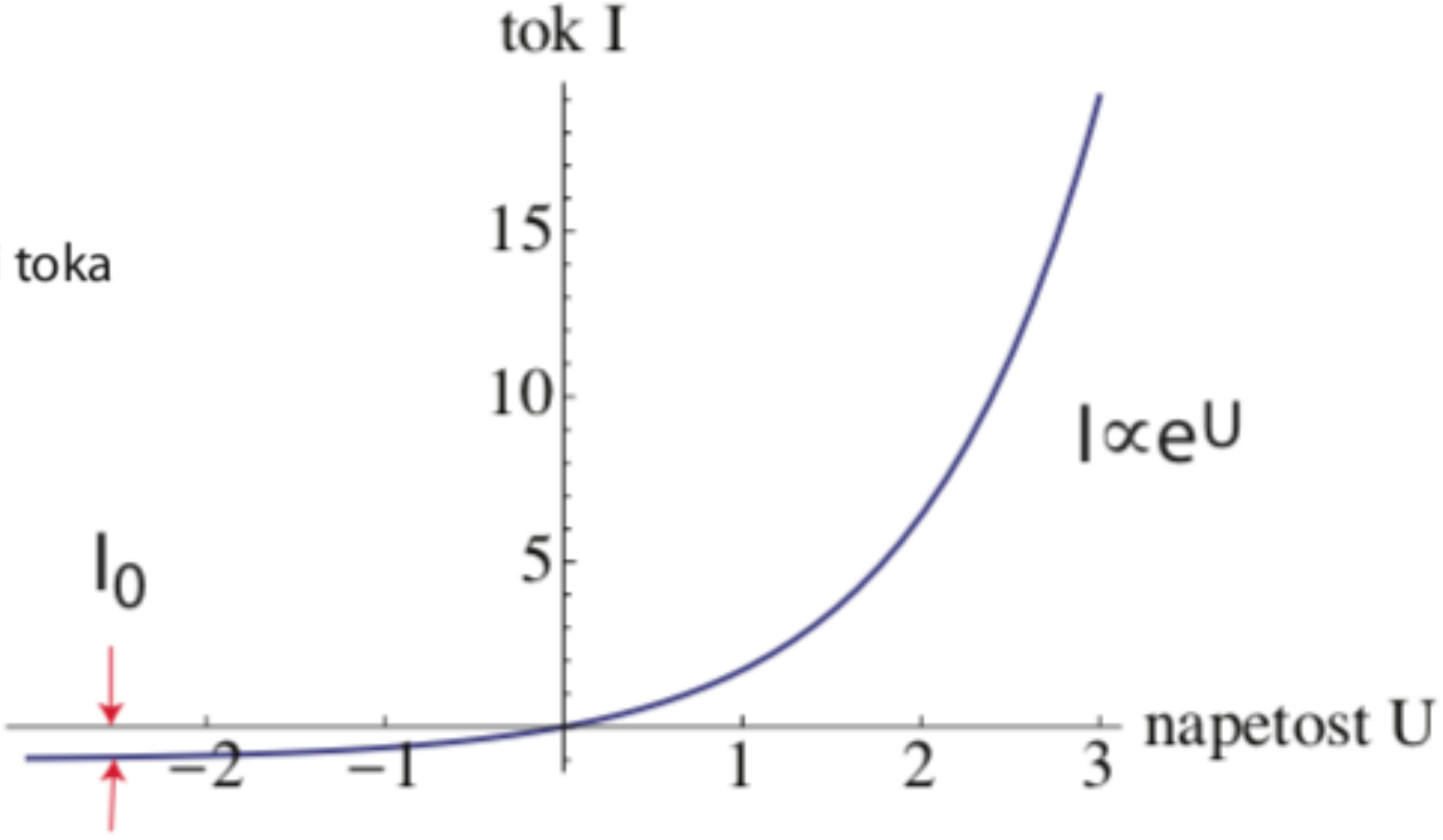


tok teče

$$I = I_0 \left(\mathrm{e}^{\frac{e_0 U}{k_B T}} - 1 \right)$$

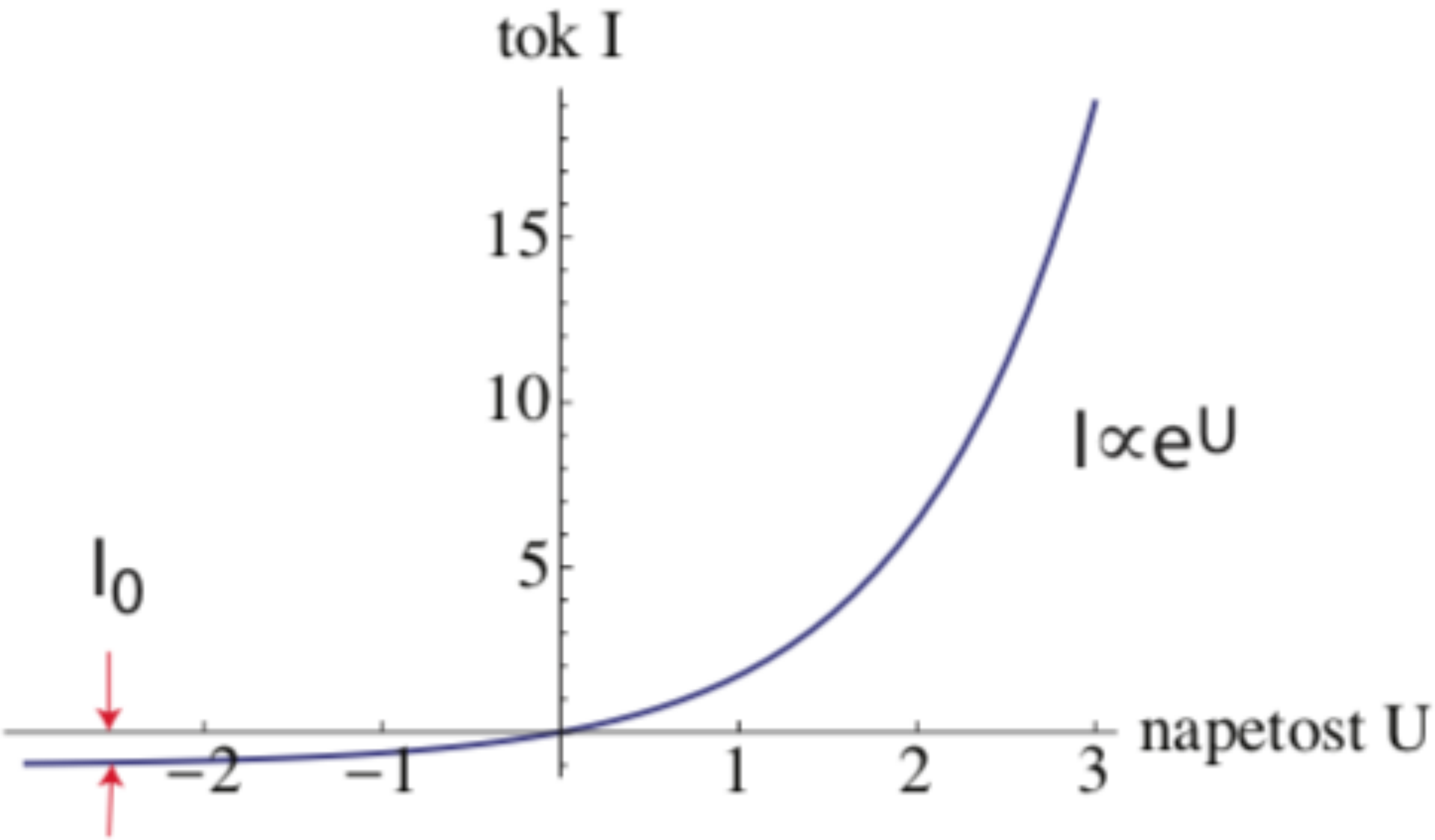


ni toka



tok zasičenja

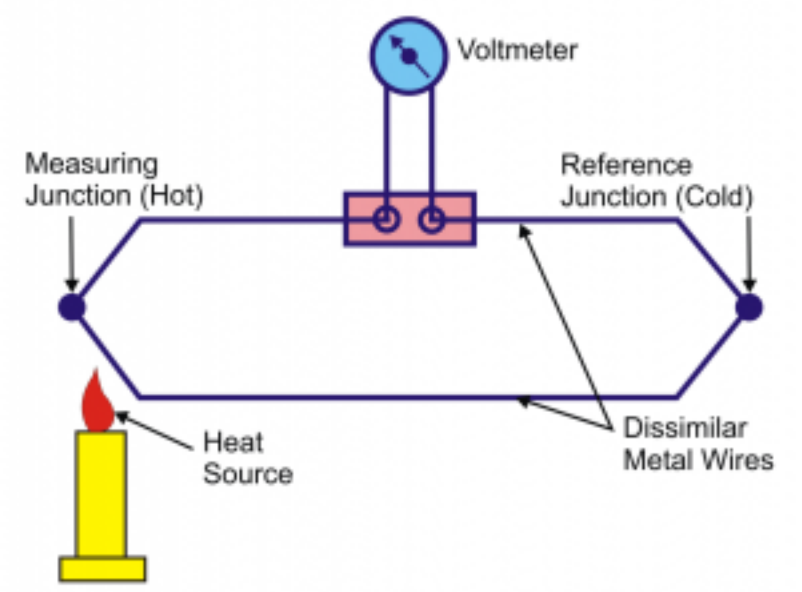
$$I = I_0 \left(e^{\frac{e_0 U}{k_B T}} - 1 \right)$$

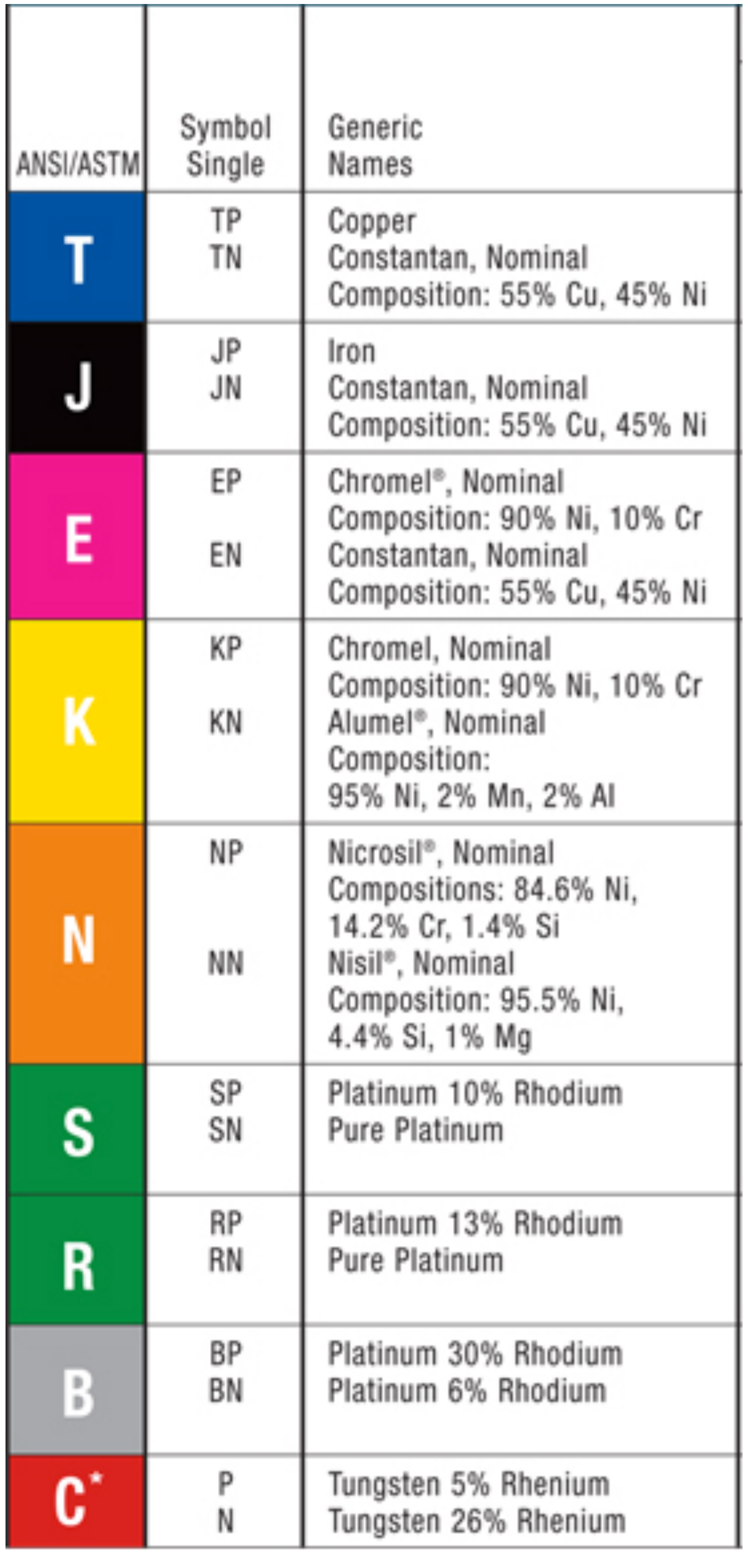


termistor

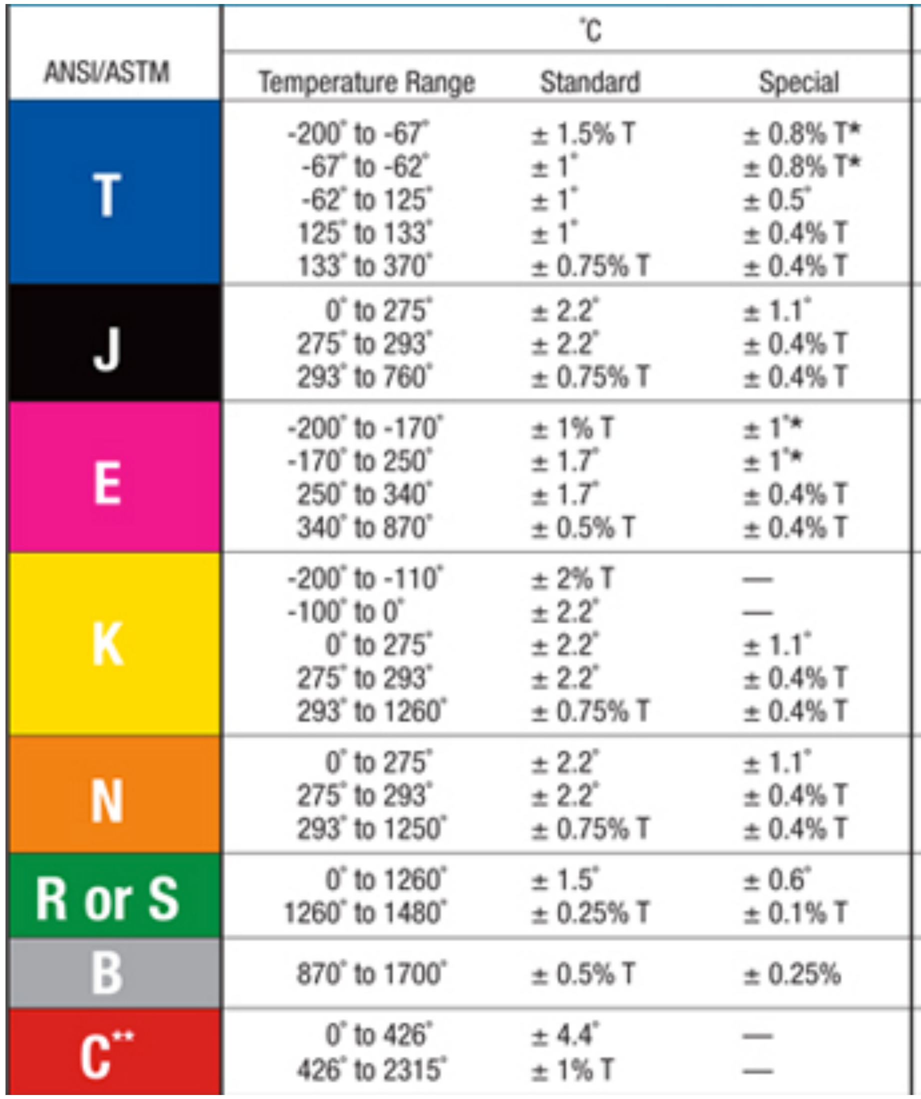
$$\alpha_T = \frac{1}{R(T)}\frac{dR}{dT}.$$

termočlen



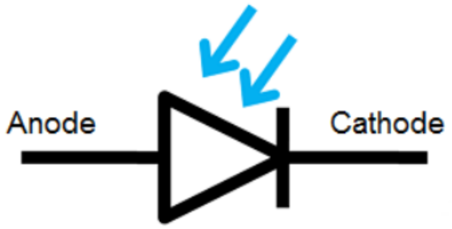


ANSI/ASTM	Symbol Single	Generic Names
T	TP TN	Copper Constantan, Nominal Composition: 55% Cu, 45% Ni
J	JP JN	Iron Constantan, Nominal Composition: 55% Cu, 45% Ni
E	EP EN	Chromel®, Nominal Composition: 90% Ni, 10% Cr Constantan, Nominal Composition: 55% Cu, 45% Ni
K	KP KN	Chromel, Nominal Composition: 90% Ni, 10% Cr Alumel®, Nominal Composition: 95% Ni, 2% Mn, 2% Al
N	NP NN	Nicrosil®, Nominal Compositions: 84.6% Ni, 14.2% Cr, 1.4% Si Nisil®, Nominal Composition: 95.5% Ni, 4.4% Si, 1% Mg
S	SP SN	Platinum 10% Rhodium Pure Platinum
R	RP RN	Platinum 13% Rhodium Pure Platinum
B	BP BN	Platinum 30% Rhodium Platinum 6% Rhodium
C*	P N	Tungsten 5% Rhenium Tungsten 26% Rhenium

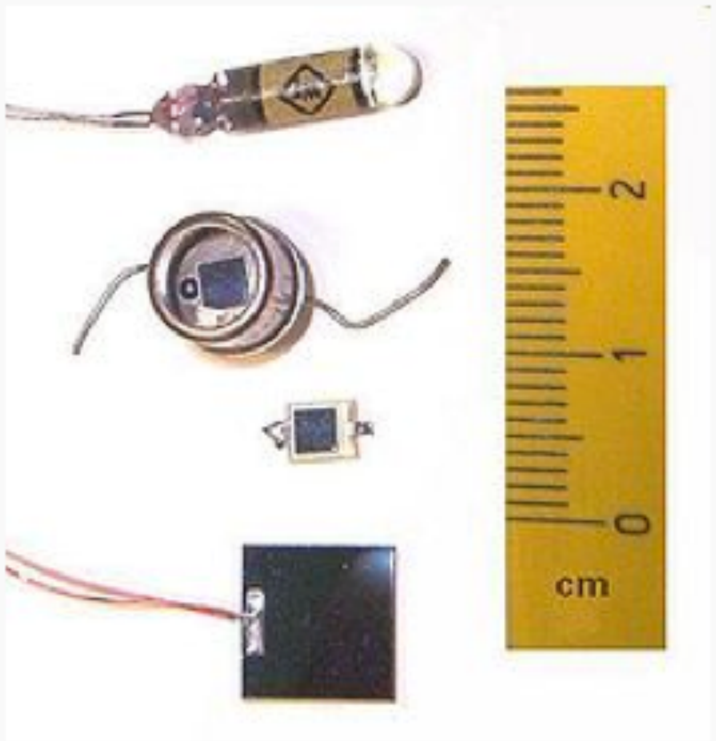


ANSI/ASTM	°C		
	Temperature Range	Standard	Special
T	-200° to -67°	± 1.5% T	± 0.8% T*
	-67° to -62°	± 1°	± 0.8% T*
	-62° to 125°	± 1°	± 0.5°
	125° to 133°	± 1°	± 0.4% T
	133° to 370°	± 0.75% T	± 0.4% T
J	0° to 275°	± 2.2°	± 1.1°
	275° to 293°	± 2.2°	± 0.4% T
	293° to 760°	± 0.75% T	± 0.4% T
E	-200° to -170°	± 1% T	± 1°*
	-170° to 250°	± 1.7°	± 1°*
	250° to 340°	± 1.7°	± 0.4% T
	340° to 870°	± 0.5% T	± 0.4% T
K	-200° to -110°	± 2% T	—
	-100° to 0°	± 2.2°	—
	0° to 275°	± 2.2°	± 1.1°
	275° to 293°	± 2.2°	± 0.4% T
	293° to 1260°	± 0.75% T	± 0.4% T
N	0° to 275°	± 2.2°	± 1.1°
	275° to 293°	± 2.2°	± 0.4% T
	293° to 1250°	± 0.75% T	± 0.4% T
R or S	0° to 1260°	± 1.5°	± 0.6°
	1260° to 1480°	± 0.25% T	± 0.1% T
B	870° to 1700°	± 0.5% T	± 0.25%
C**	0° to 426°	± 4.4°	—
	426° to 2315°	± 1% T	—

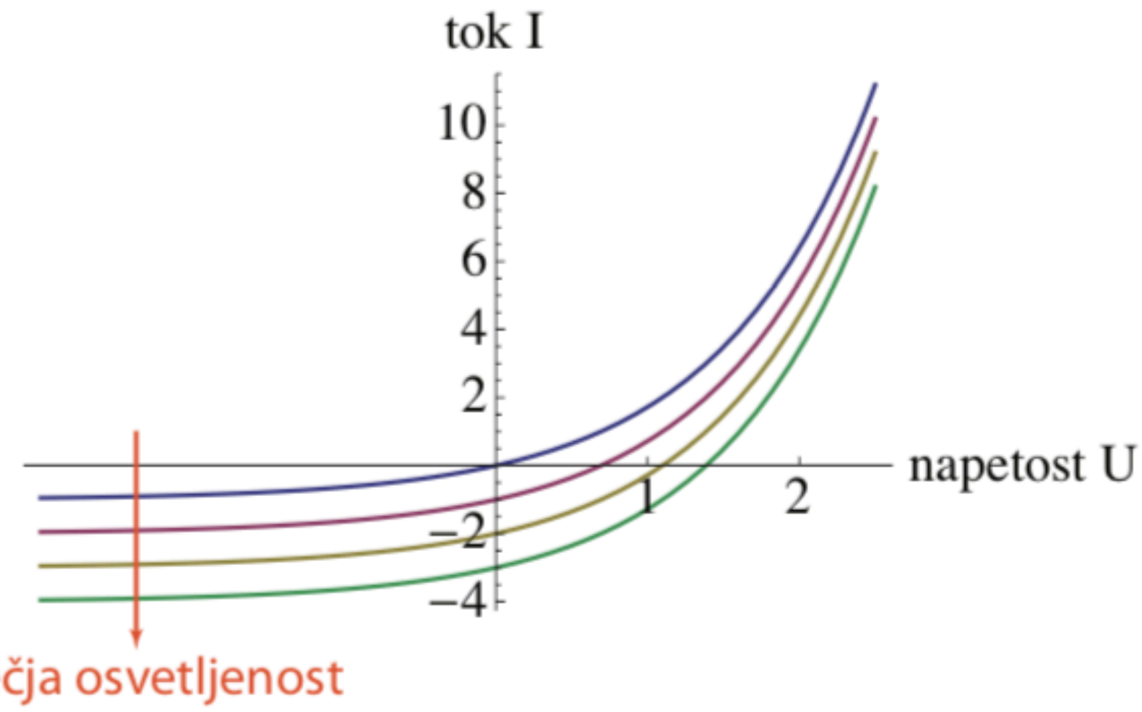
FOTODIODA

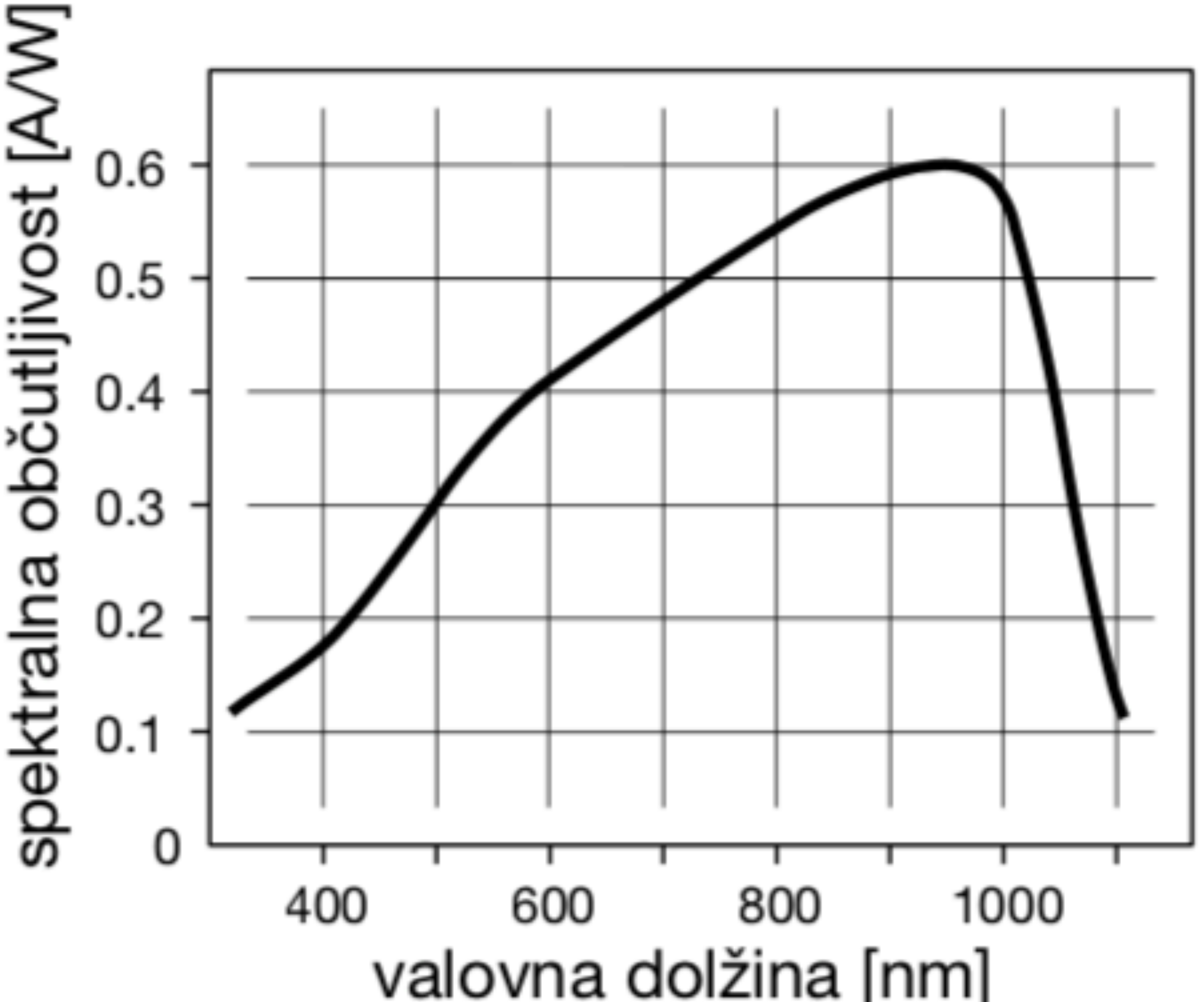


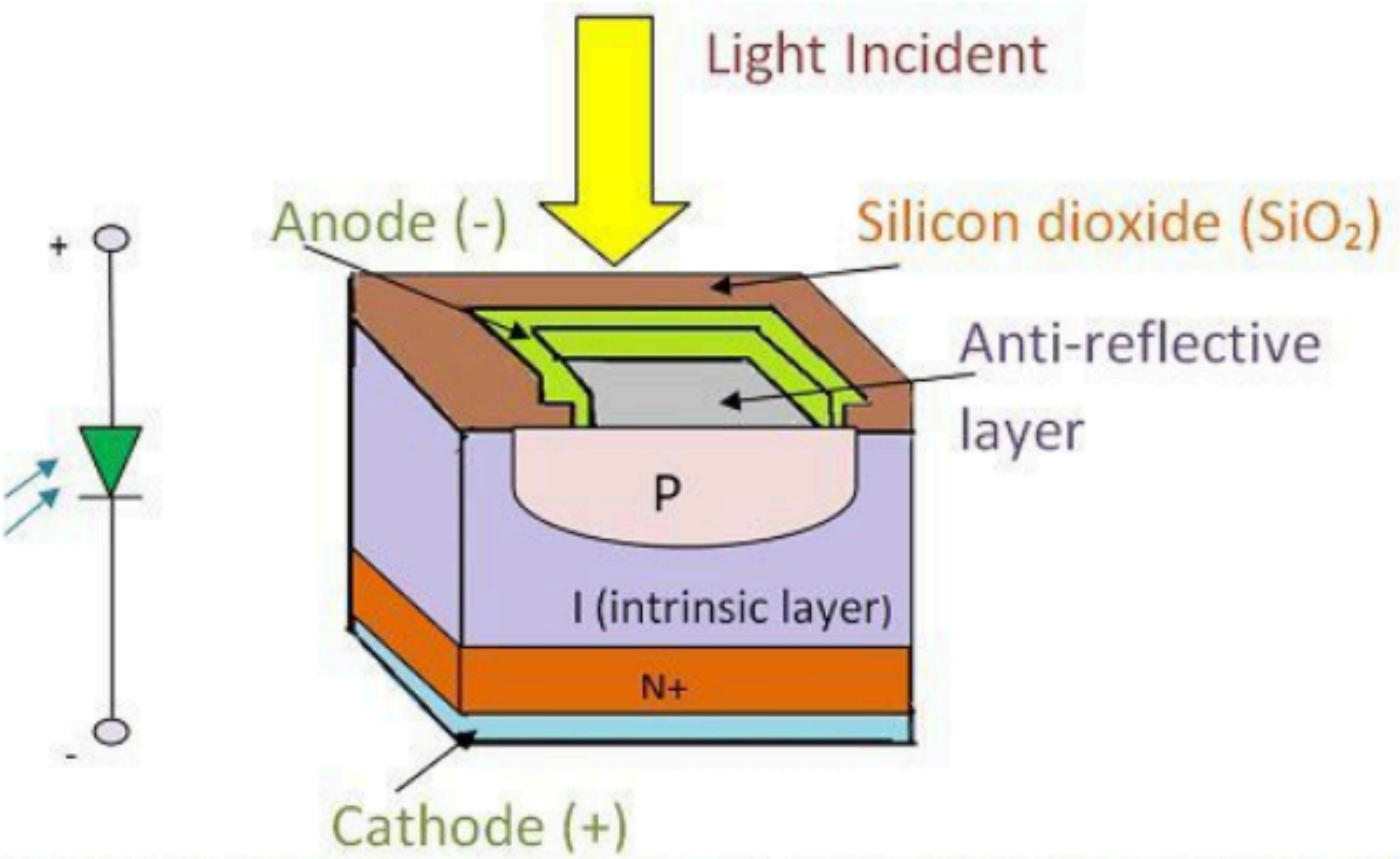
Photodiode



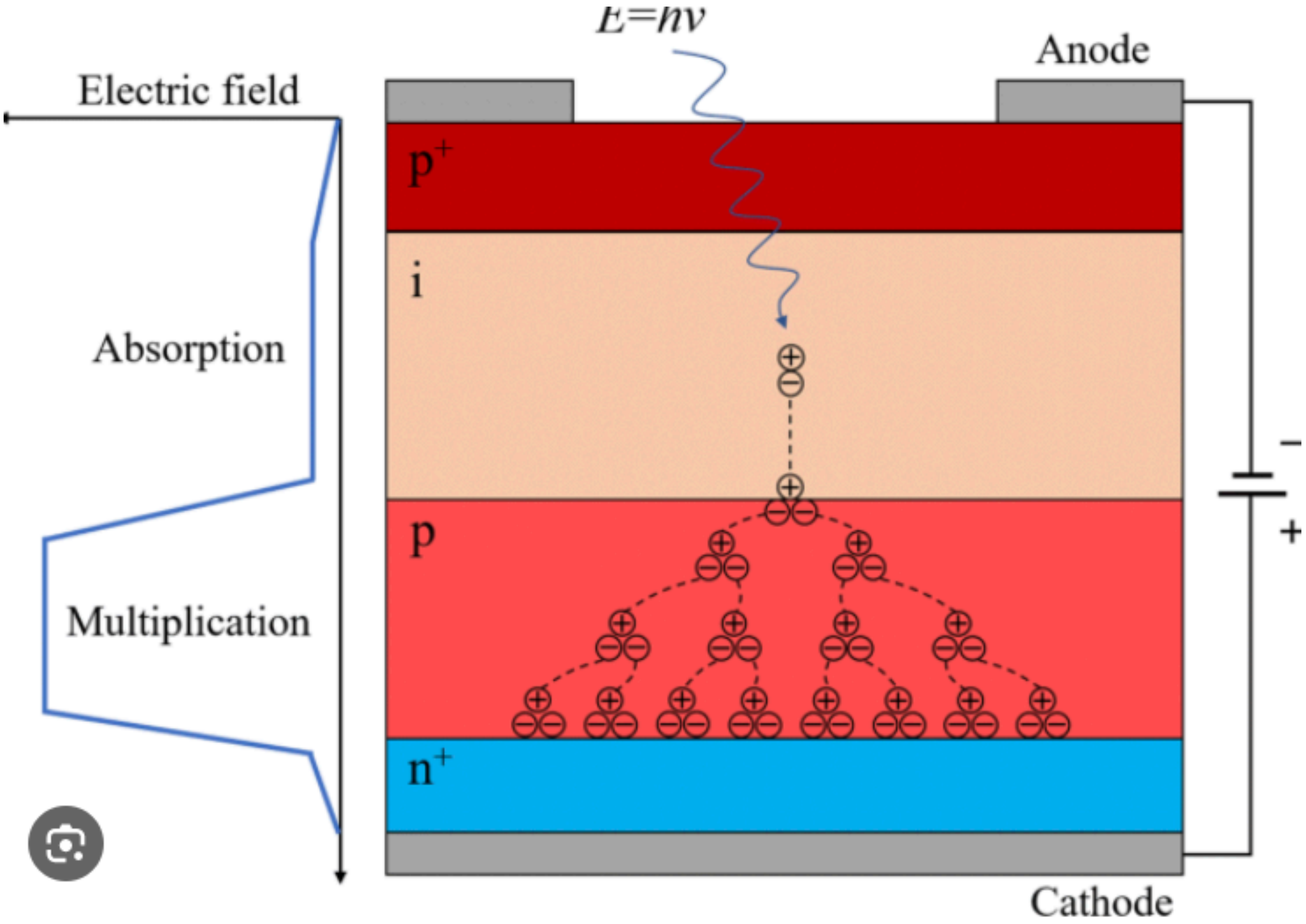
Three Si and one Ge (bottom) photodiodes.






Light Incident
Anode (-)
Silicon dioxide (SiO_2)
Anti-reflective layer
P
I (intrinsic layer)
N+
Cathode (+)
+
-

avalanche photodiode



Single Photon Detection Modules with Fixed Gain

Zoom

- Wavelength Range: 400 nm - 1000 nm
- Free-Space or FC/PC Connector Versions
- Maximum Dark Count Rate: 100 Hz or 250 Hz
- High Photon Detection Efficiency (See Table to the Right)
- Ø100 µm Active Detector (Nominal)

These SPDMHx Single Photon Detector Modules feature high photon detection efficiencies (PDEs) that extend into the NIR and low dark count rates, enabled by combining ultra-low-noise silicon avalanche photodiodes with specially developed quenching and signal processing electronics. Incoming photons generate corresponding electrical pulses that are converted into TTL pulses at the LEMO connector output. A LEMO to BNC adapter is included.

Versions are available with a maximum dark count rate of 100 Hz (Item #s SPDMH2 and SPDMH2F) or 250 Hz (Item #s SPDMH3 and SPDMH3F).

The detectors can be purchased in a free-space version (Item #s SPDMH2 or SPDMH3) that has internal SM1 (1.035"-40) threading for compatibility with Ø1" lens tubes. We also offer versions with an FC/PC fiber optic receptacle that is pre-aligned to the detector, allowing a multimode fiber optic patch cable to be directly connected to the input (Item #s SPDMH2F or SPDMH3F).

For flexible integration into optical systems, there is an 8-32 tapped hole on each side of the input. The base plate of the detector can be mounted directly to an optical table or breadboard using CL4 Table Clamps. Alternatively, three Ø3.9 mm (Ø0.15") through holes on each side of the base plate accept 6-32 screws for compatibility with the BA4 mounting base. For the free-space detectors, we recommend mounting the BA4 mounting base to a 3-Axis translation stage or other positioning stage to enable precise alignment.

In order to avoid damage to the module, adequate heat sinking must be provided by placing or mounting the module onto a suitable heat sink, e.g. an optical table, breadboard or base plate. Avoid stray light impinging on the detector, which affects the count rate. Employ appropriate shielding for the SPDMH2 and SPDMH3 free space models and make sure that any optical fiber assembly attached to the FC/PC connector of the SPDMH2F or SPDMH3F modules shields unwanted light.

A power supply with a region-specific plug is included with each module.

Item #	**SPDMH2[a]**	**SPDMH2F[a]**	**SPDMH3[a]**	**SPDMH3F[a]**
Detector				
Detector Type	Si Avalanche Photodetector			
Wavelength Range	400 nm - 1000 nm			
Photon Detection Efficiency				
Active Detector Size[b]	Ø100 µm (Nominal)			
Typical Photon Detection Efficiency[c]	10% @ 405 nm 50% @ 520 nm 70% @ 670 nm 60% @ 810 nm			
Dark Count Rate (Max)	100 Hz		250 Hz	
Count Rate	20 MHz (Max)			
Input Fiber Compatibility				
Fiber Connector	N/A	FC/PC	N/A	FC/PC
Input Fiber Core Diameter (Max)	N/A	<105 µm	N/A	<105 µm
Numerical Aperture	N/A	≤0.29	N/A	≤0.29

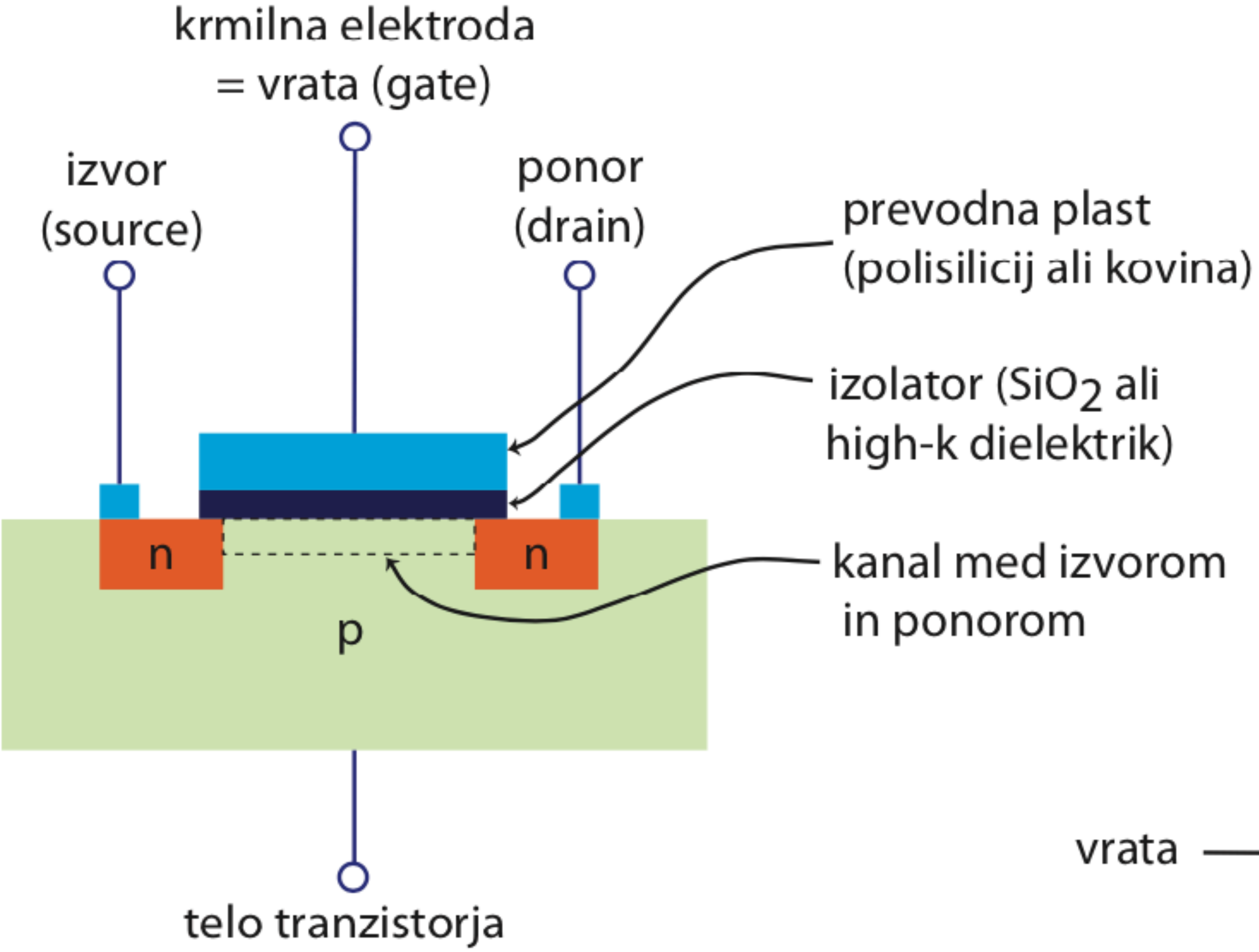
a. See the *Specs* tab for complete specifications.
b. The active area of the integrated Si Avalanche Photodetector is larger than 100 µm. The SPDMH2F and SPDMH3F modules are optimized for optical fibers as specified above. A pre-aligned GRIN lens focuses the light onto a spot of <70 µm diameter in the center of the detector.
c. Specifications are valid for modules without the FC/PC connector.

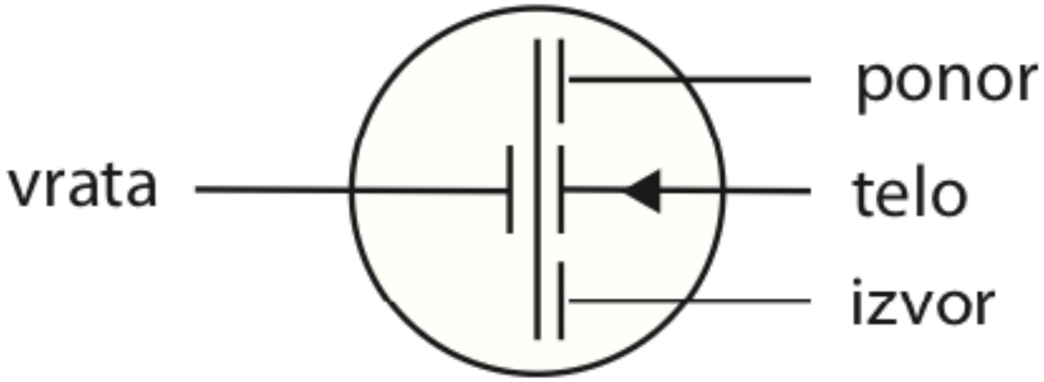
Based on your currency / country selection, your order will ship from Munich, Germany

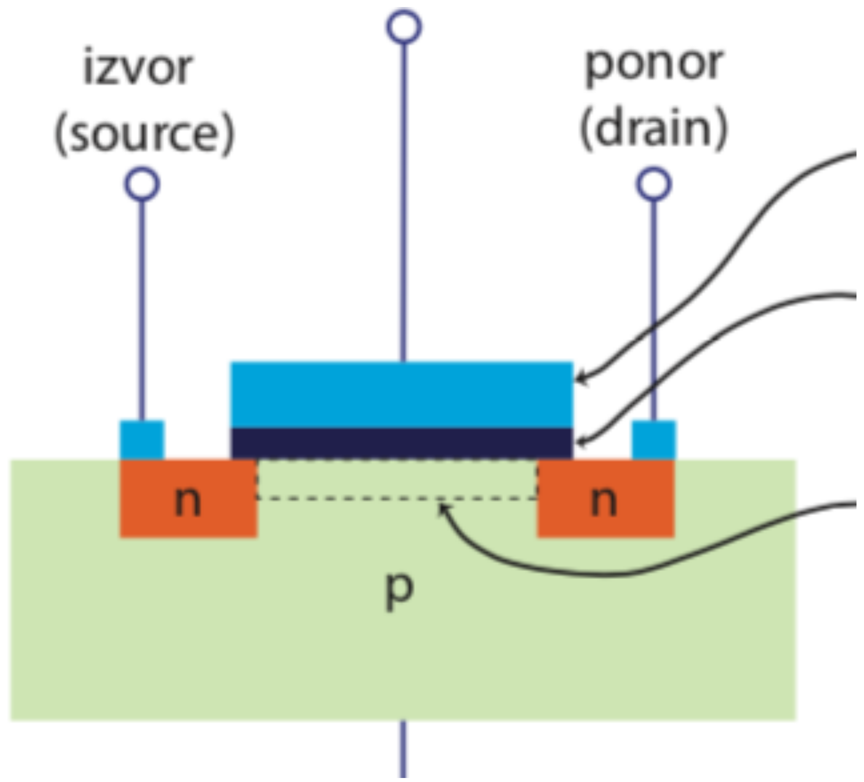
+1	**Qty**	**Docs**	**Part Number - Universal**		**Price ex VAT**	**Available**
+1			**SPDMH2**	Single Photon Detection Module, 400 - 1000 nm, Ø100 µm Active Area, 100 Hz Dark Count Rate	5.072,90 €	Today
+1			**SPDMH2F**	Single Photon Detection Module, 400 - 1000 nm, Ø100 µm Active Area, 100 Hz Dark Count Rate, FC/PC Connector	5.521,49 €	Today
+1			**SPDMH3**	Single Photon Detection Module, 400 - 1000 nm, Ø100 µm Active Area, 250 Hz Dark Count Rate	4.118,45 €	Today
+1			**SPDMH3F**	Single Photon Detection Module, 400 - 1000 nm, Ø100 µm Active Area, 250 Hz Dark Count Rate, FC/PC Connector	4.872,47 €	Today

Add To Cart

tranzistor na poljski pojav






izvor
(source)
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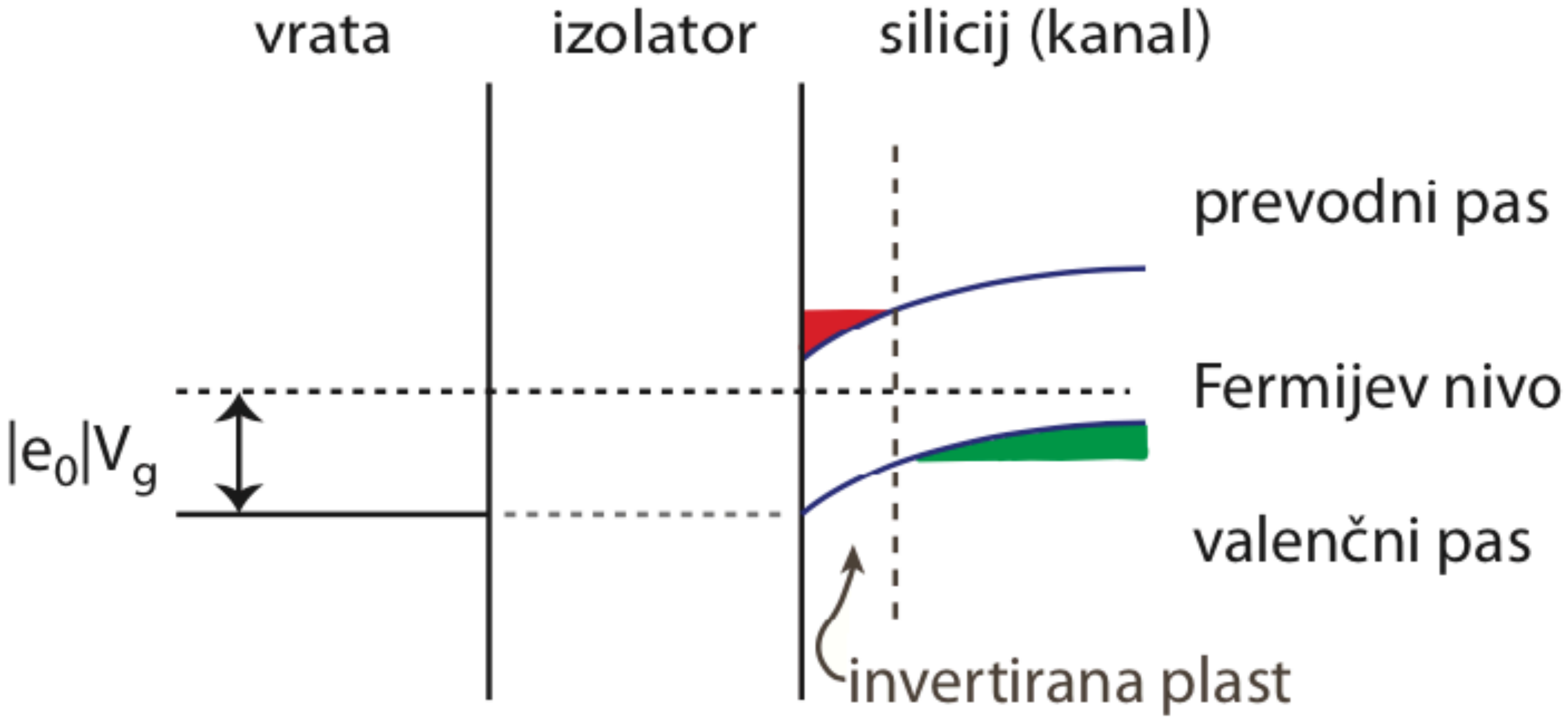
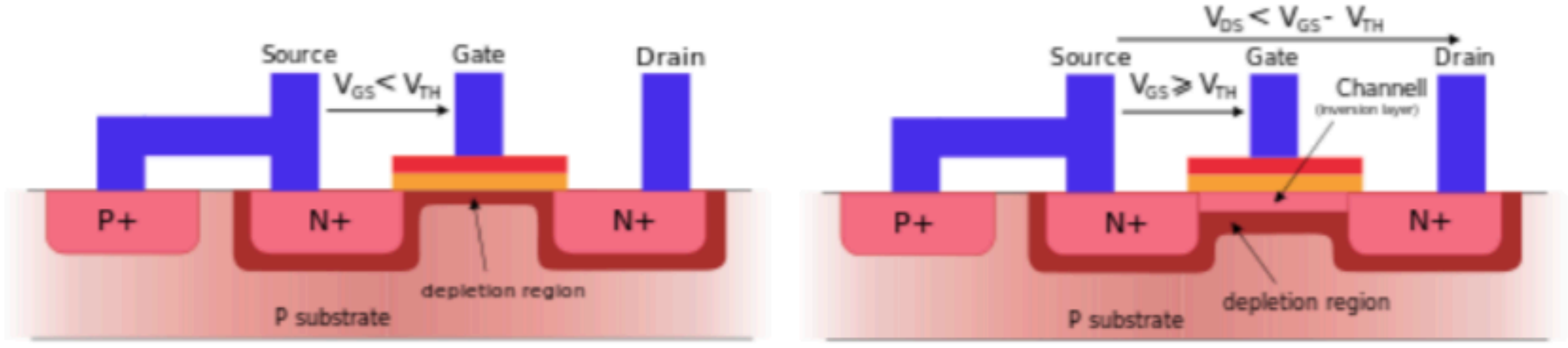
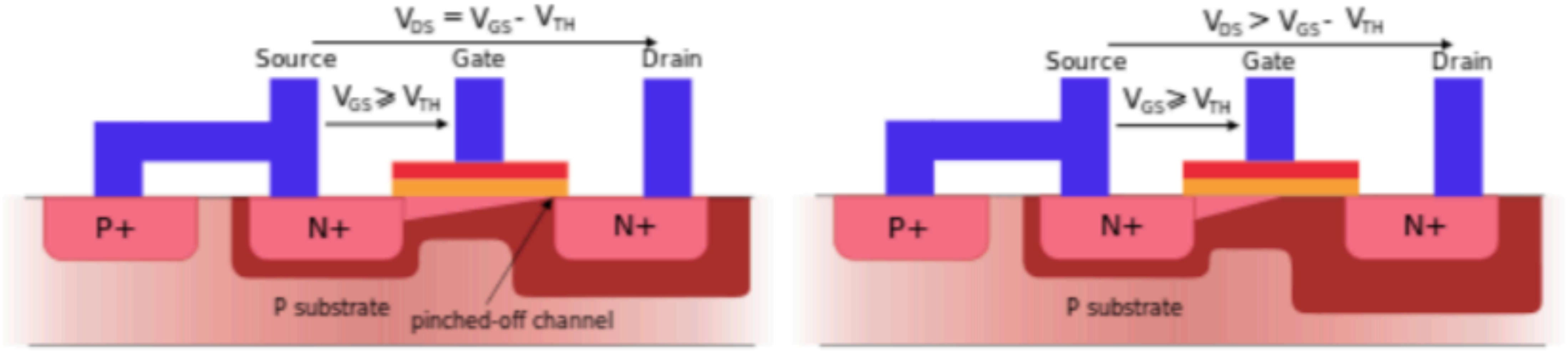

vrata
izolator
silicij (kanal)
prevodni pas
Fermijev nivo
valenčni pas
$|e_0|V_g$
invertirana plast



Linear operating region (ohmic mode)

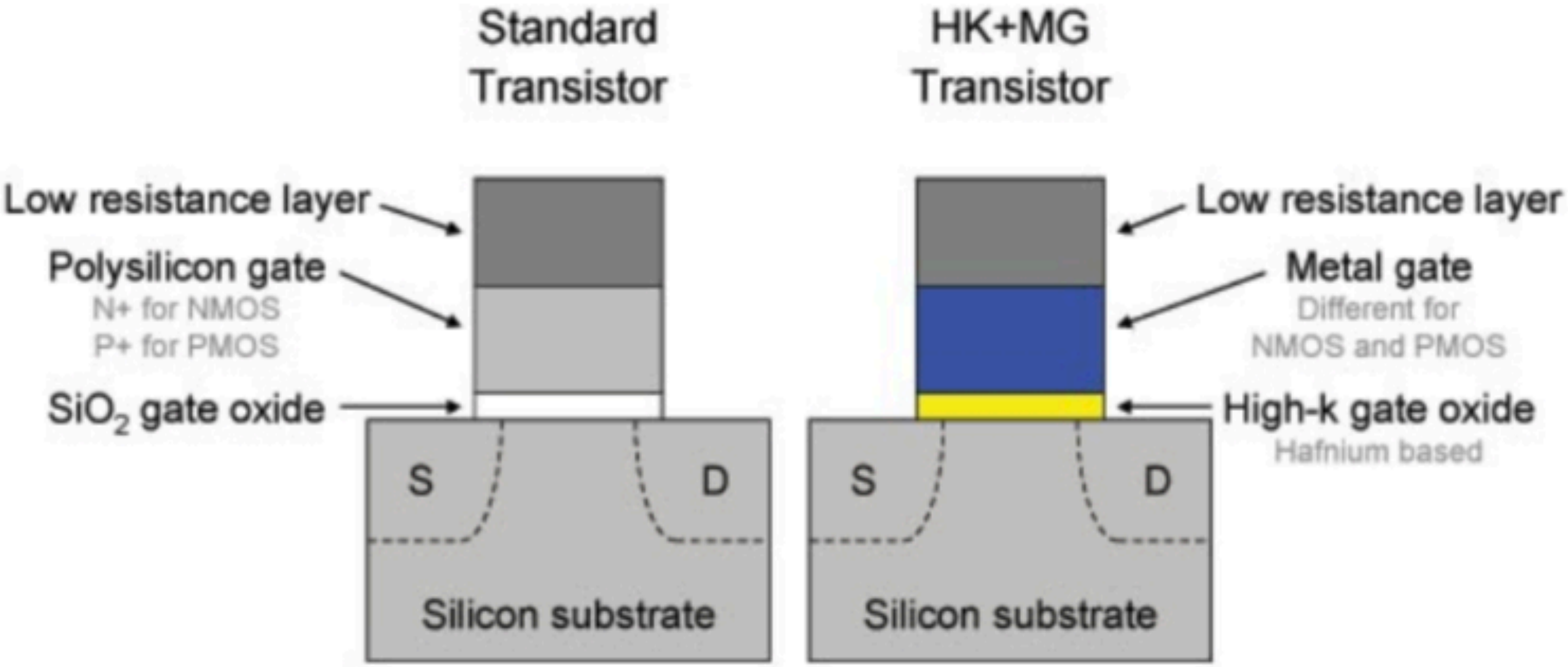


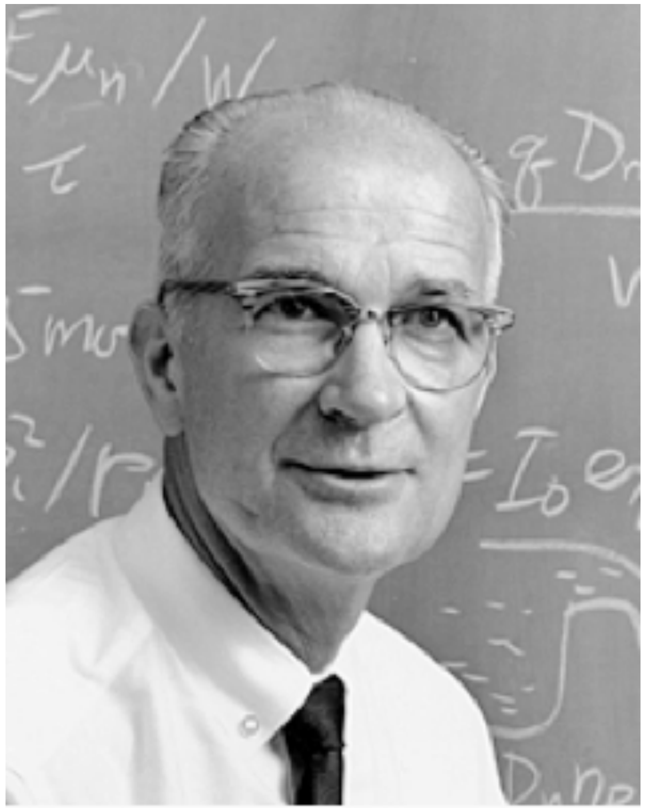
Saturation mode at point of pinch-off

Saturation mode

MOSFET Functioning / Olivier Deleage & Peter Scott / CC BY SA

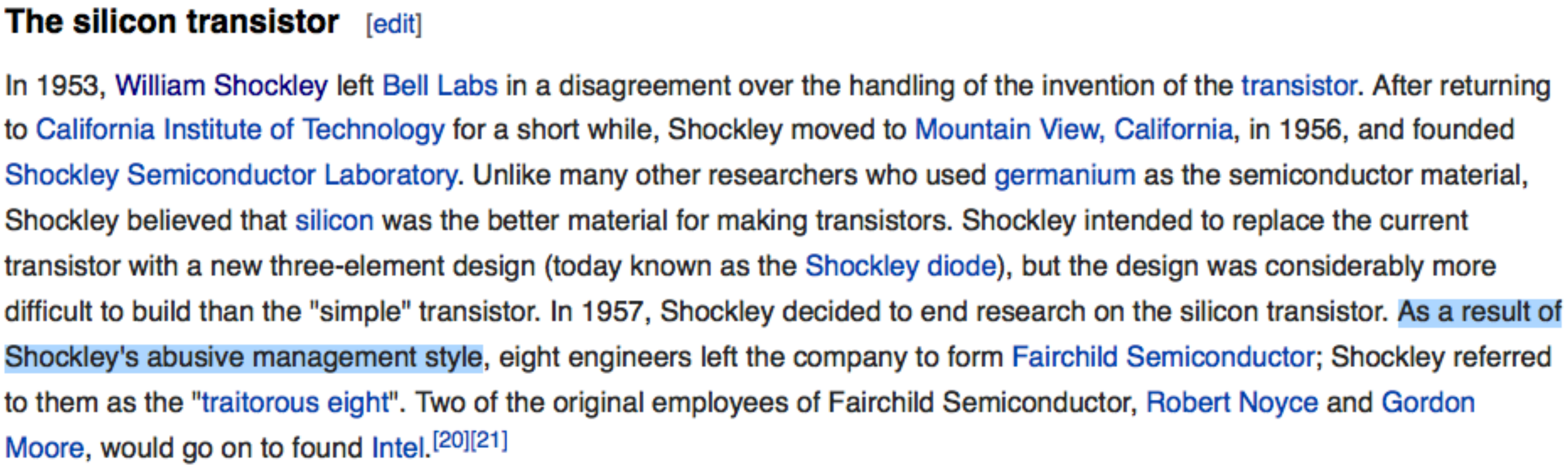
High-k/Metal Gate





W. Shockley (1910-1989)

Nobelova 1956 (izum tranzistorja, skupaj z Brattainom in Bardeenom)



The silicon transistor [edit]

In 1953, William Shockley left Bell Labs in a disagreement over the handling of the invention of the transistor. After returning to California Institute of Technology for a short while, Shockley moved to Mountain View, California, in 1956, and founded Shockley Semiconductor Laboratory. Unlike many other researchers who used germanium as the semiconductor material, Shockley believed that silicon was the better material for making transistors. Shockley intended to replace the current transistor with a new three-element design (today known as the Shockley diode), but the design was considerably more difficult to build than the "simple" transistor. In 1957, Shockley decided to end research on the silicon transistor. As a result of Shockley's abusive management style, eight engineers left the company to form Fairchild Semiconductor; Shockley referred to them as the "traitorous eight". Two of the original employees of Fairchild Semiconductor, Robert Noyce and Gordon Moore, would go on to found Intel.[20][21]

Traitorous eight

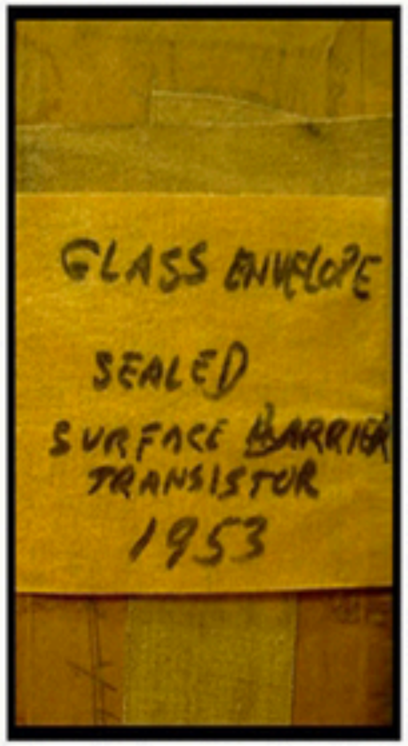
From Wikipedia, the free encyclopedia

From left to right: Gordon Moore, C. Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni and Jay Last. (1960)

The **traitorous eight** are eight men who left Shockley Semiconductor Laboratory in 1957. William Shockley had in 1956 recruited a group of young PhD graduates with the goal to develop and produce new semiconductor devices. While Shockley had received a Nobel Prize in Physics and was an experienced researcher and teacher, his managing of the group created harsh working conditions.[note 1] He chose a strategy for circuit design that failed and created an intolerable working atmosphere.[note 2] The group of PhD graduates hired demanded that Shockley be replaced. When their demands were rebuffed, they realized they had to leave.

Shockley described their leaving as a "betrayal". The eight who left Shockley Semiconductor were Julius Blank, Victor Grinich, Jean Hoerni, Eugene Kleiner, Jay Last, Gordon Moore, Robert Noyce and Sheldon Roberts. In August 1957 they reached an agreement with Sherman Fairchild and on September 18, 1957 they formed Fairchild Semiconductor. The newly founded Fairchild Semiconductor soon grew into a leader of the semiconductor industry. In 1960 it became an incubator of Silicon Valley, and was directly or indirectly involved in the creation of dozens of corporations such as AMD and Intel.[1] These many spin-off companies came to be known as "Fairchildren".

1953 “Experimental” Philco Surface Barrier Transistor



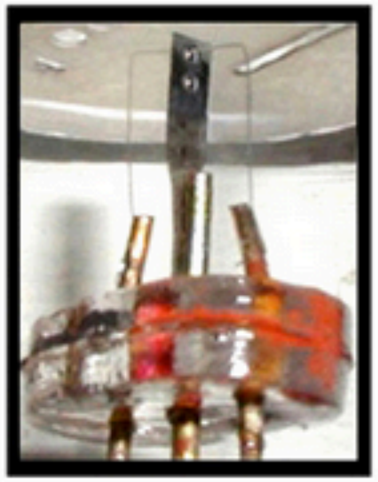
GLASS ENVELOPE
SEALED
SURFACE BARRIER
TRANSISTOR
1953

Original hand-written description information on outside of tube box

“Experimental” Transistor

Philco Marked

Production Model Actual Size

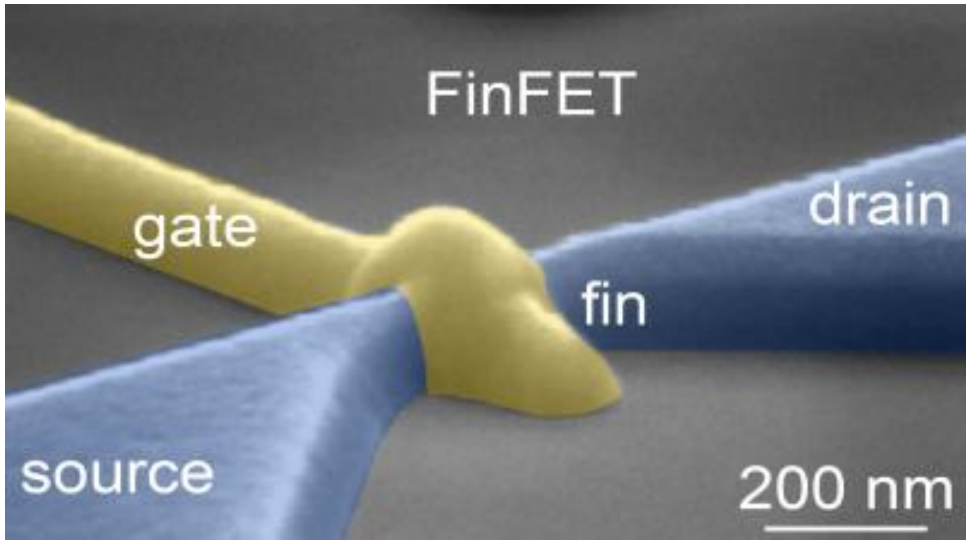


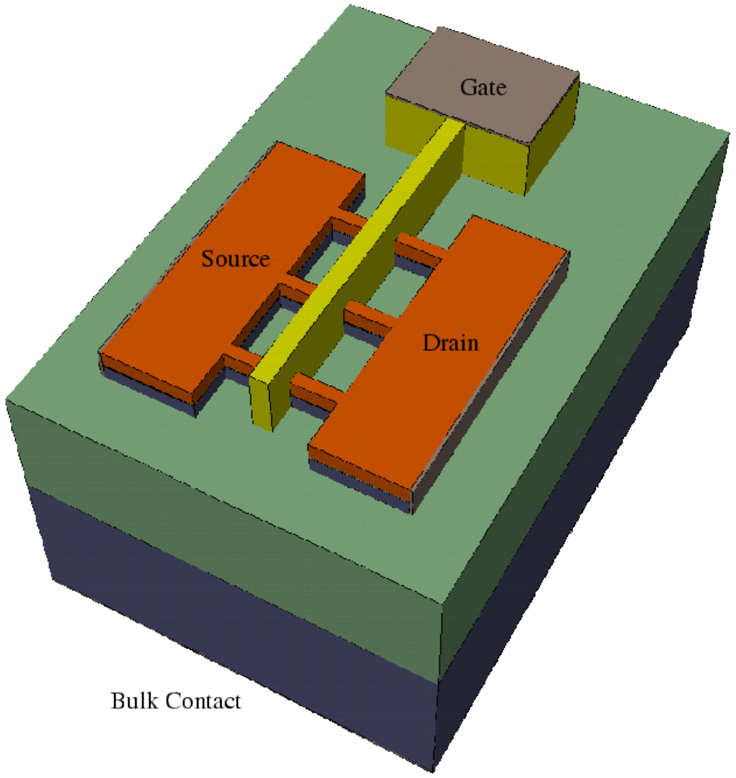
Close-Up View Surface Barrier Transistor

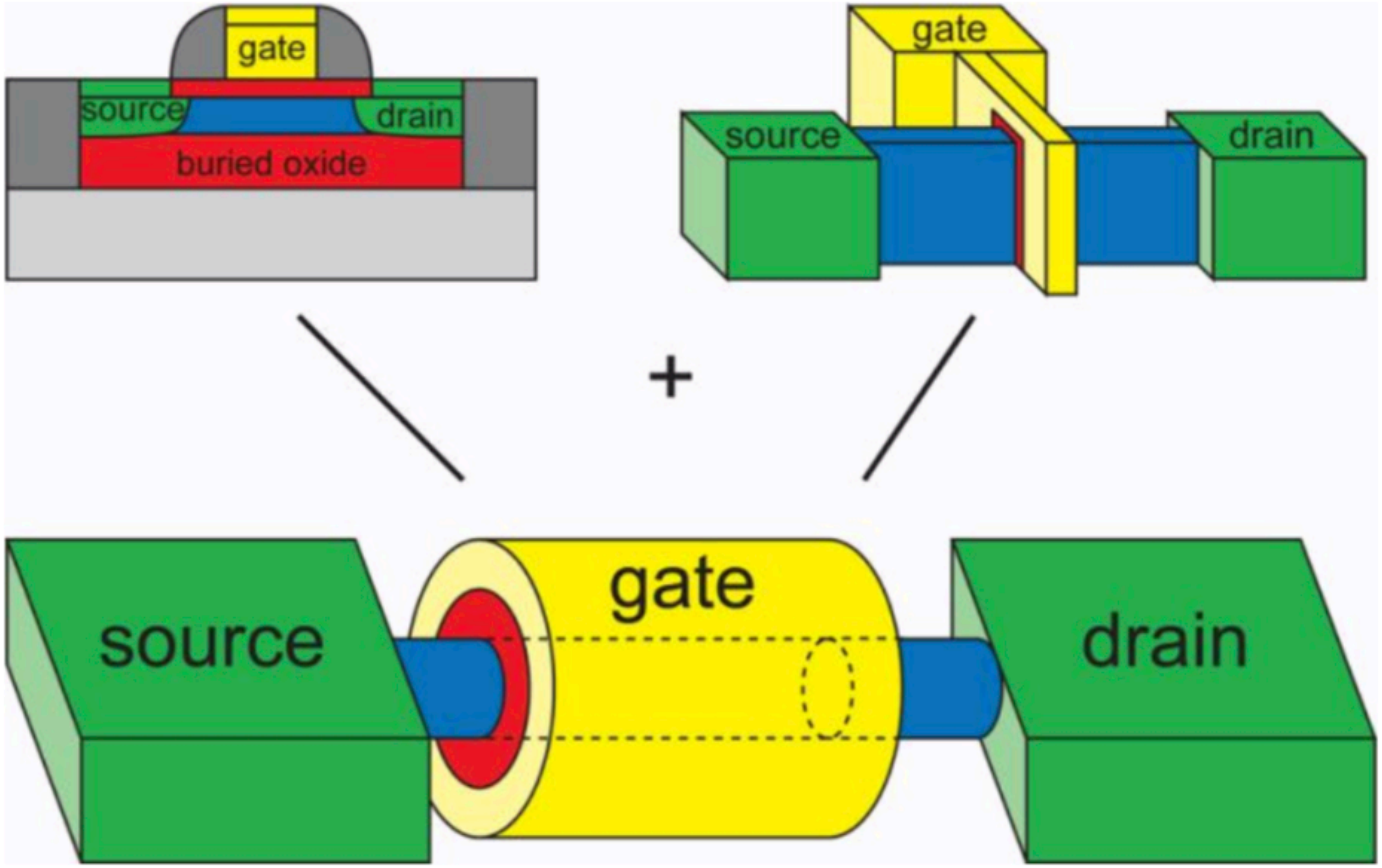
Production Model Enlarged View

FinFET, MUGFET

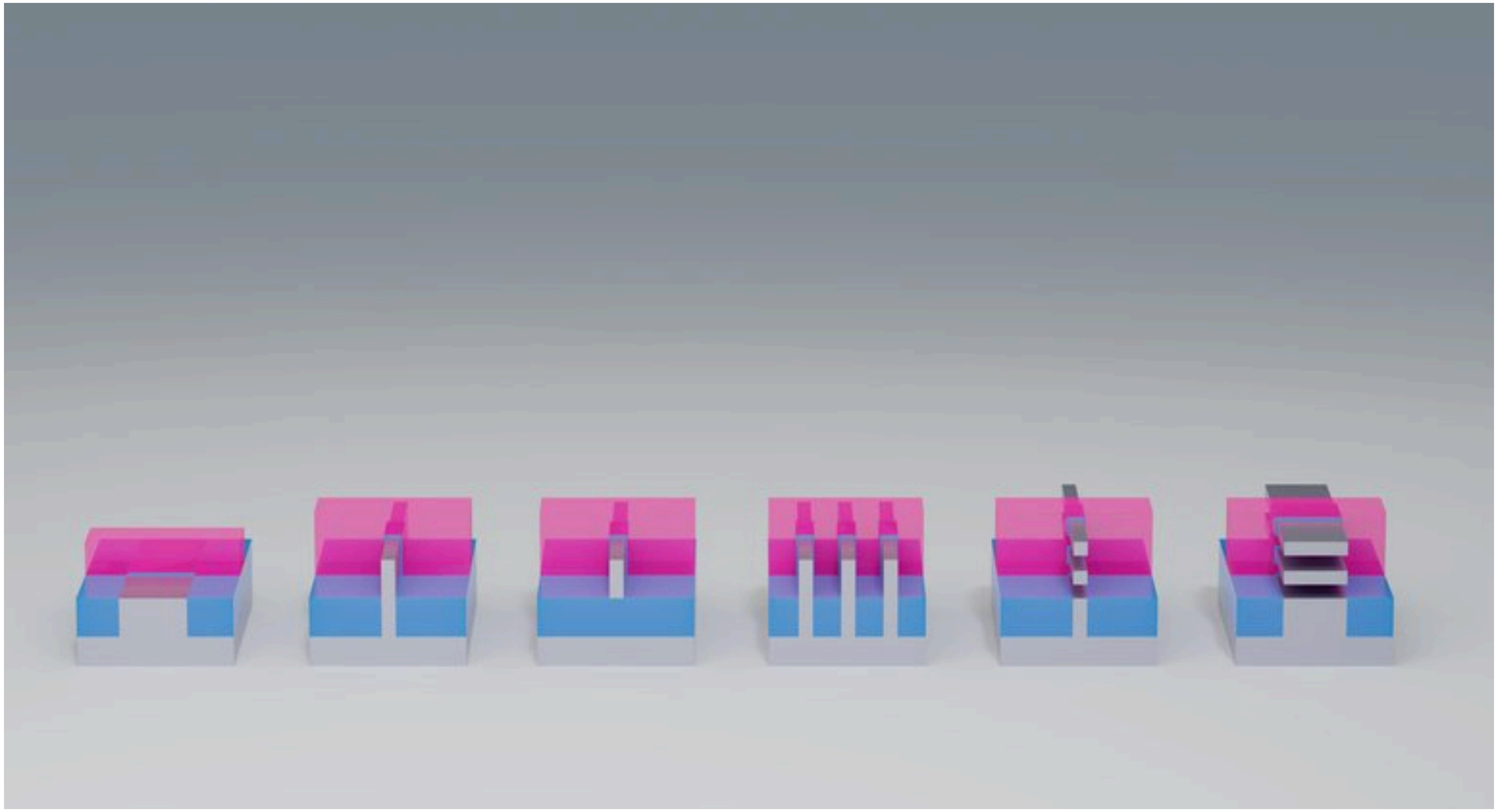
multiple gate

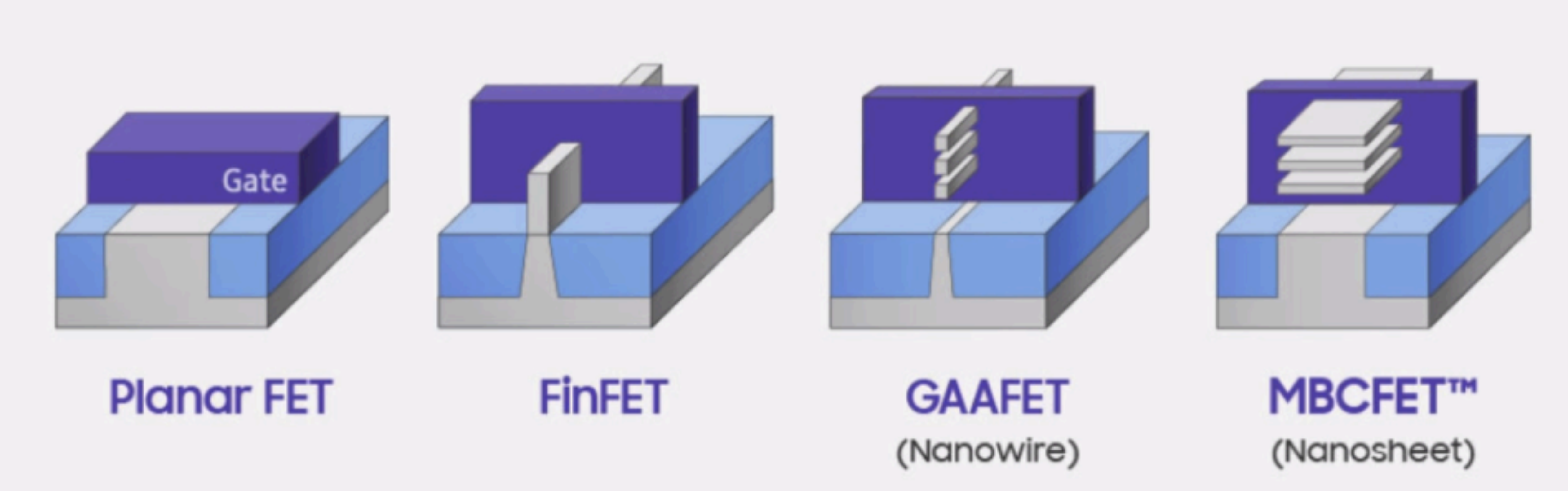


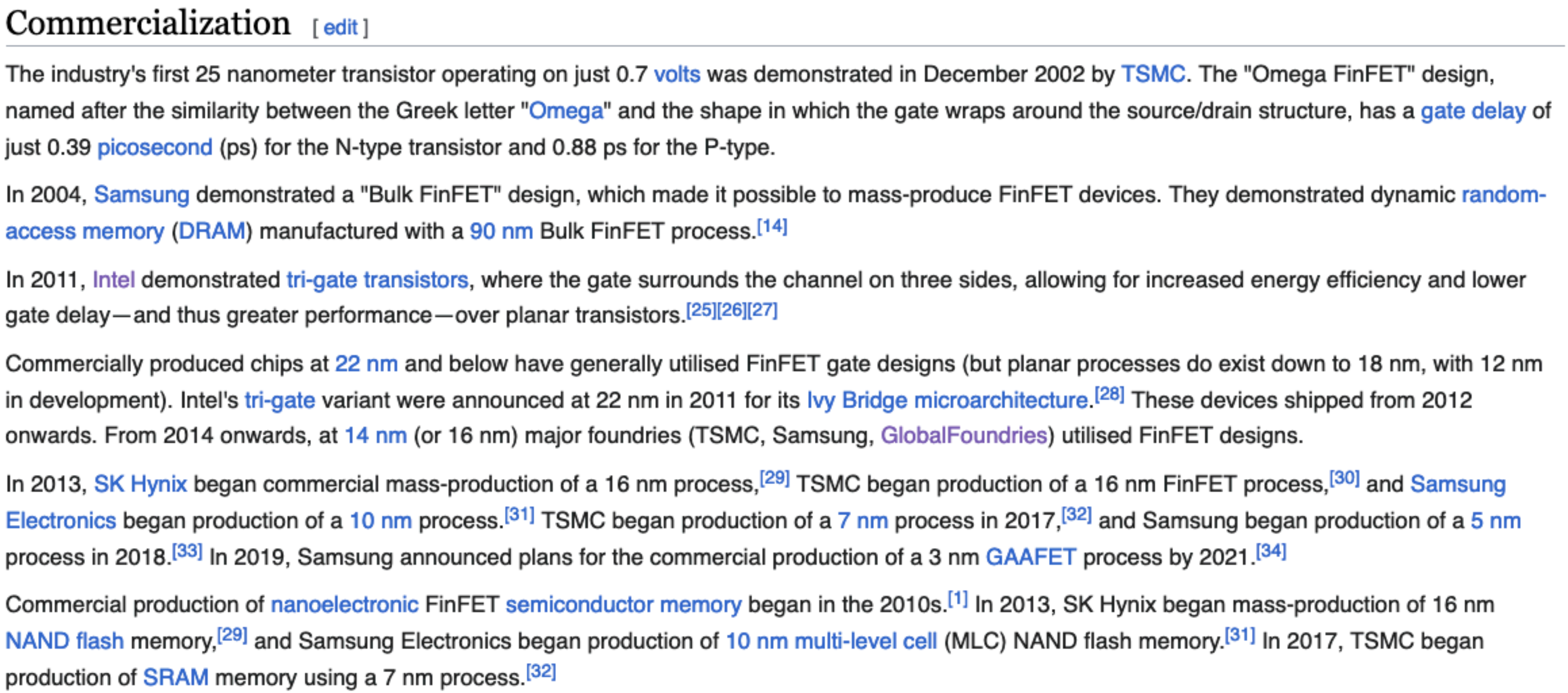




CNFET / Joerg Appenzeller




Gate
Planar FET
FinFET
GAAFET
(Nanowire)
MBCFET™
(Nanosheet)



Commercialization [edit]

The industry's first 25 nanometer transistor operating on just 0.7 volts was demonstrated in December 2002 by TSMC. The "Omega FinFET" design, named after the similarity between the Greek letter "Omega" and the shape in which the gate wraps around the source/drain structure, has a gate delay of just 0.39 picosecond (ps) for the N-type transistor and 0.88 ps for the P-type.

In 2004, Samsung demonstrated a "Bulk FinFET" design, which made it possible to mass-produce FinFET devices. They demonstrated dynamic random-access memory (DRAM) manufactured with a 90 nm Bulk FinFET process.[14]

In 2011, Intel demonstrated tri-gate transistors, where the gate surrounds the channel on three sides, allowing for increased energy efficiency and lower gate delay—and thus greater performance—over planar transistors.[25][26][27]

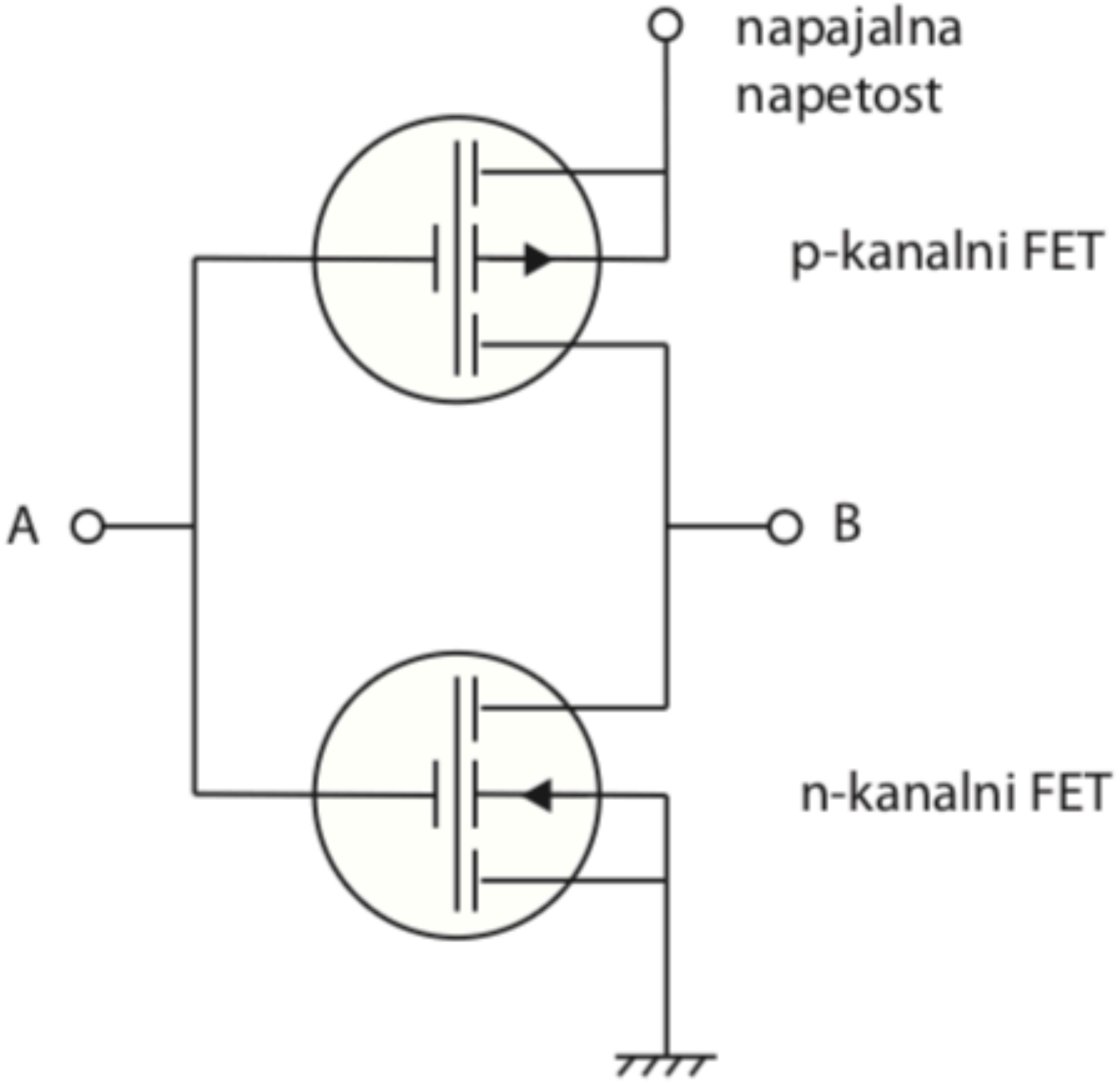
Commercially produced chips at 22 nm and below have generally utilised FinFET gate designs (but planar processes do exist down to 18 nm, with 12 nm in development). Intel's tri-gate variant were announced at 22 nm in 2011 for its Ivy Bridge microarchitecture.[28] These devices shipped from 2012 onwards. From 2014 onwards, at 14 nm (or 16 nm) major foundries (TSMC, Samsung, GlobalFoundries) utilised FinFET designs.

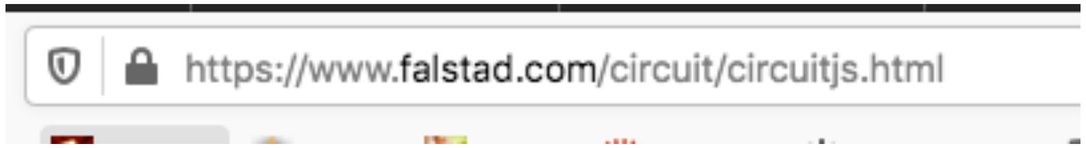
In 2013, SK Hynix began commercial mass-production of a 16 nm process,[29] TSMC began production of a 16 nm FinFET process,[30] and Samsung Electronics began production of a 10 nm process.[31] TSMC began production of a 7 nm process in 2017,[32] and Samsung began production of a 5 nm process in 2018.[33] In 2019, Samsung announced plans for the commercial production of a 3 nm GAAFET process by 2021.[34]

Commercial production of nanoelectronic FinFET semiconductor memory began in the 2010s.[1] In 2013, SK Hynix began mass-production of 16 nm NAND flash memory,[29] and Samsung Electronics began production of 10 nm multi-level cell (MLC) NAND flash memory.[31] In 2017, TSMC began production of SRAM memory using a 7 nm process.[32]

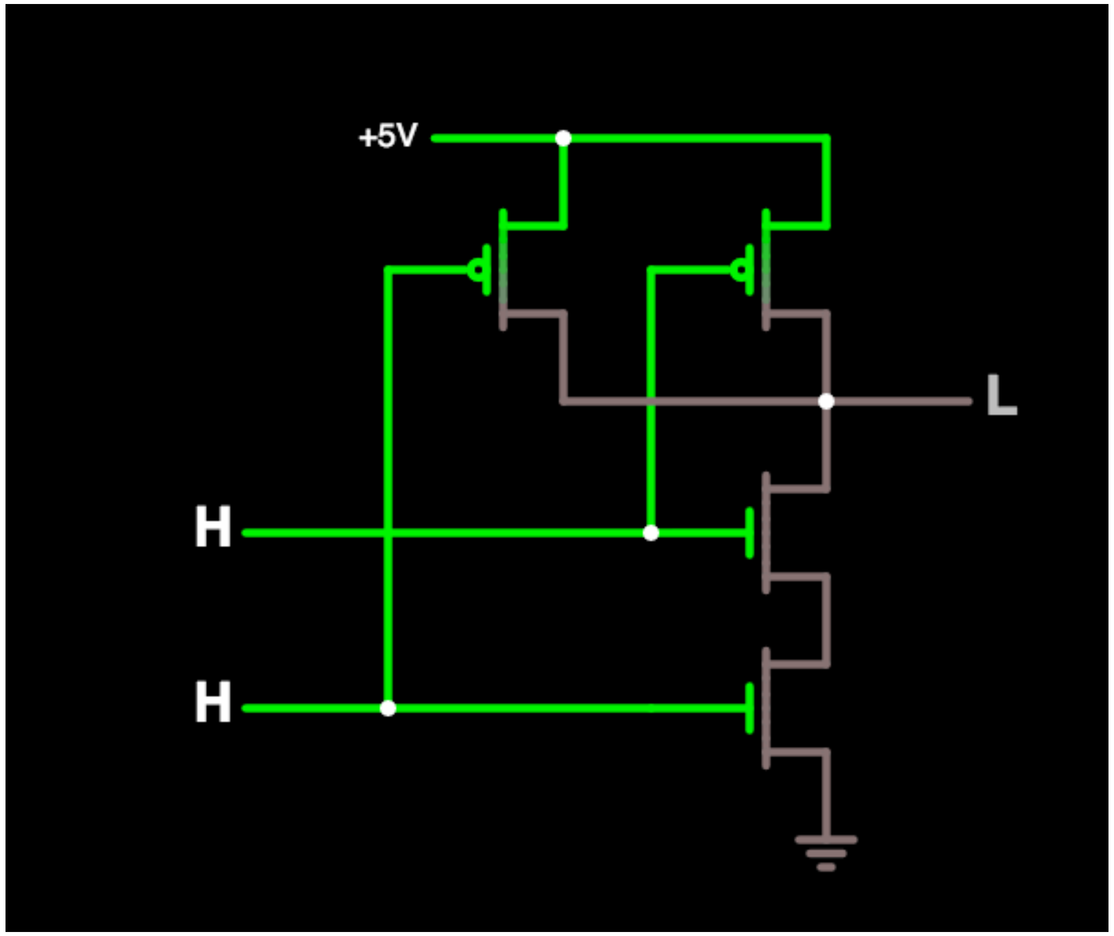
logična vrata v tehnologiji CMOS

CMOS = arhitektura in tehnologija izdelave

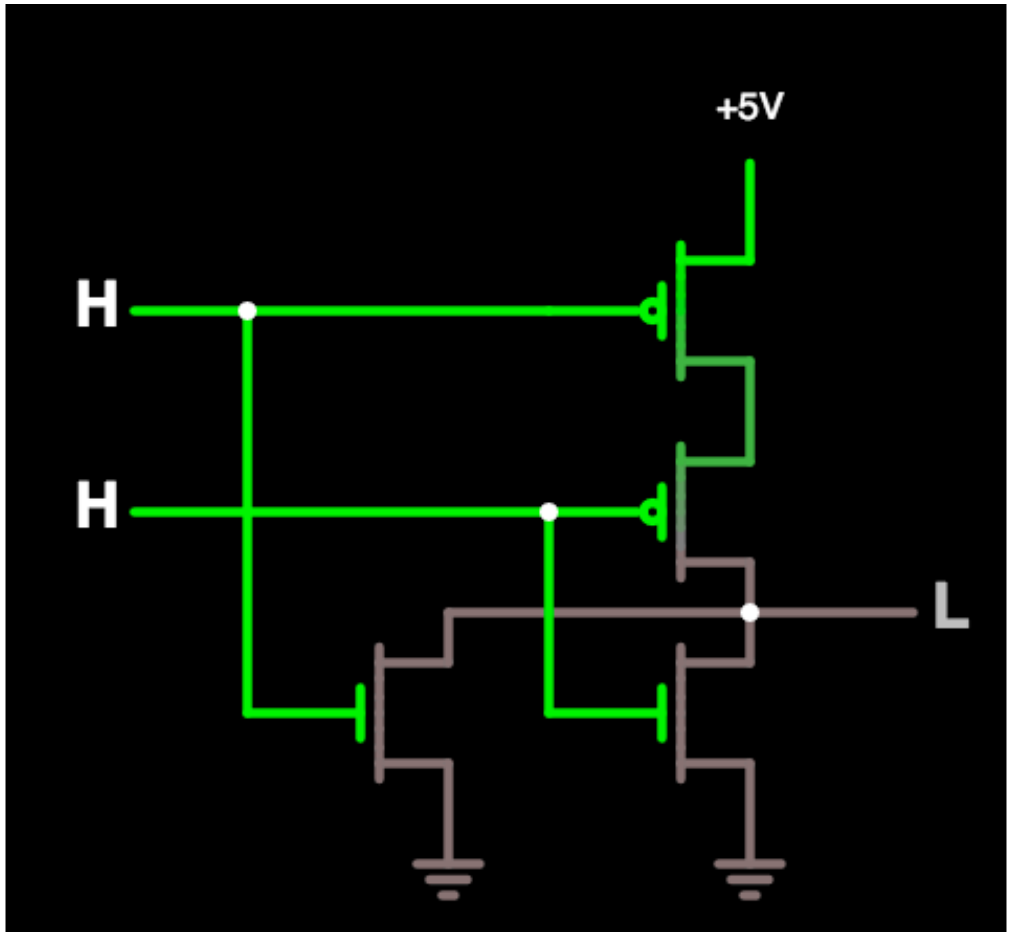




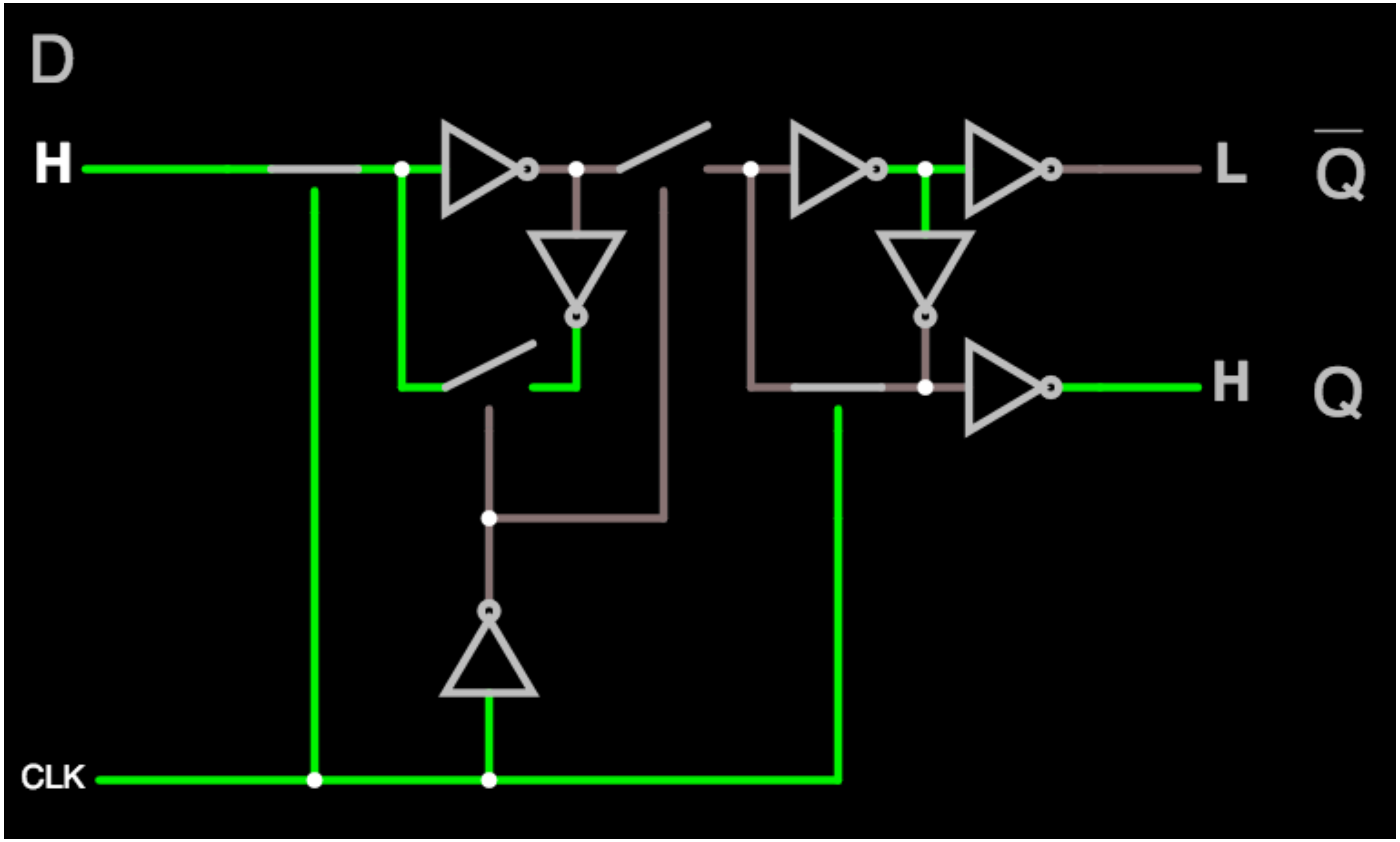
https://www.falstad.com/circuit/circuitjs.html



NAND

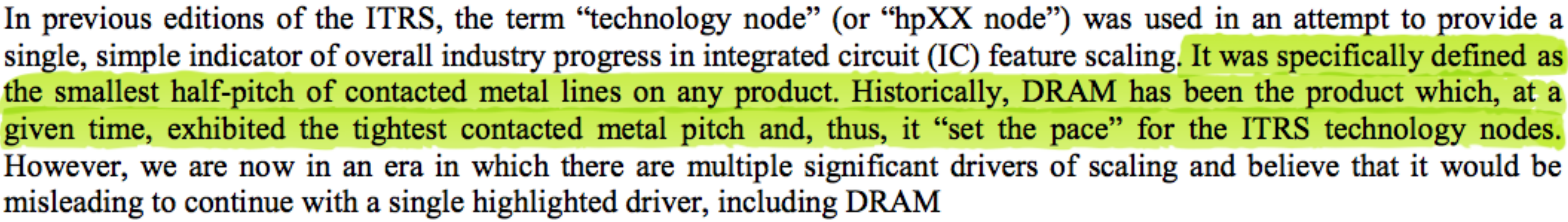


NOR



flip flop

TEHNOLOŠKI VOZEL



In previous editions of the ITRS, the term "technology node" (or "hpXX node") was used in an attempt to provide a single, simple indicator of overall industry progress in integrated circuit (IC) feature scaling. It was specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product which, at a given time, exhibited the tightest contacted metal pitch and, thus, it "set the pace" for the ITRS technology nodes. However, we are now in an era in which there are multiple significant drivers of scaling and believe that it would be misleading to continue with a single highlighted driver, including DRAM

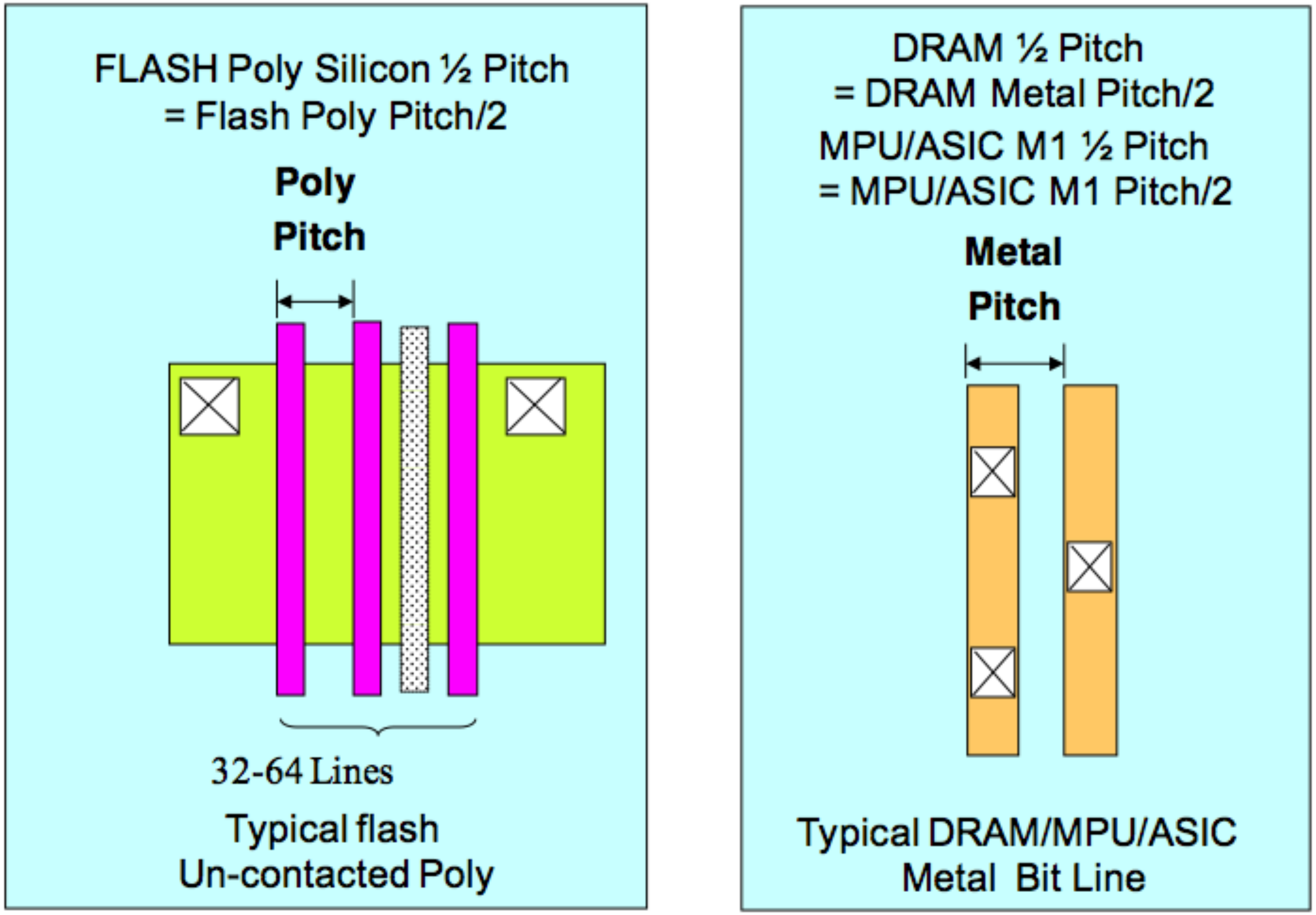


Figure 1 *2011 Definition of Pitches*

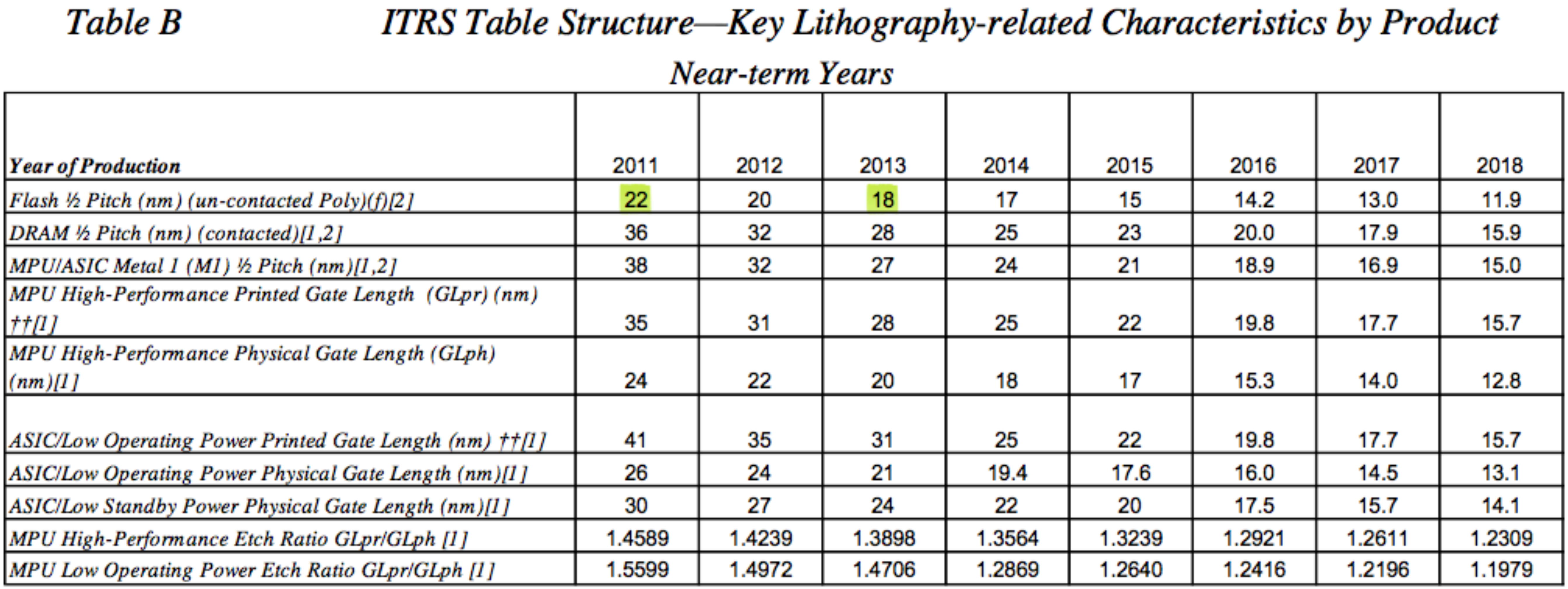


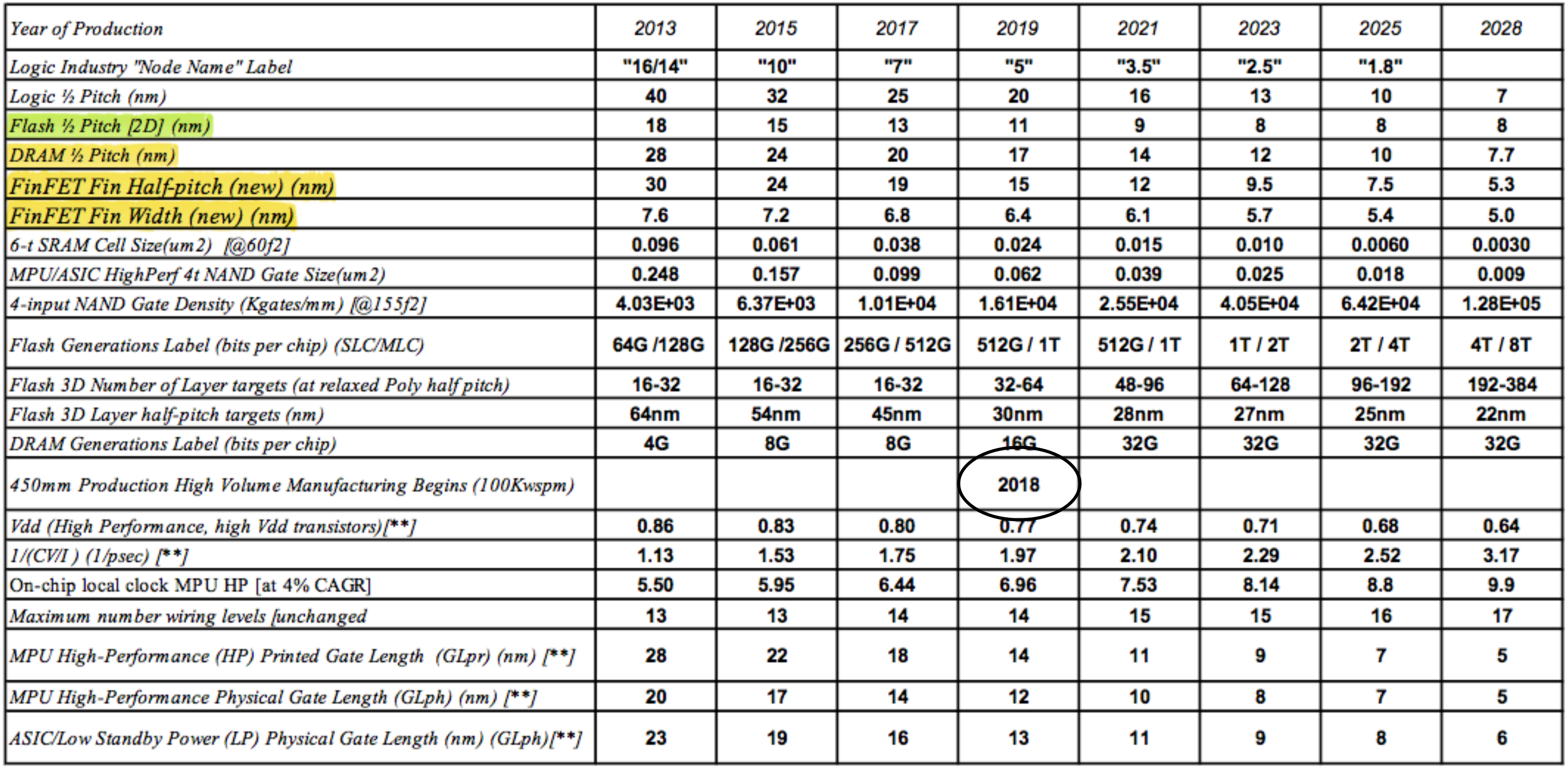
Table B *ITRS Table Structure—Key Lithography-related Characteristics by Product*

Near-term Years

Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	22	20	18	17	15	14.2	13.0	11.9
DRAM ½ Pitch (nm) (contacted)[1,2]	36	32	28	25	23	20.0	17.9	15.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	38	32	27	24	21	18.9	16.9	15.0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	35	31	28	25	22	19.8	17.7	15.7
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	24	22	20	18	17	15.3	14.0	12.8
ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	41	35	31	25	22	19.8	17.7	15.7
ASIC/Low Operating Power Physical Gate Length (nm)[1]	26	24	21	19.4	17.6	16.0	14.5	13.1
ASIC/Low Standby Power Physical Gate Length (nm)[1]	30	27	24	22	20	17.5	15.7	14.1
MPU High-Performance Etch Ratio GLpr/GLph [1]	1.4589	1.4239	1.3898	1.3564	1.3239	1.2921	1.2611	1.2309
MPU Low Operating Power Etch Ratio GLpr/GLph [1]	1.5599	1.4972	1.4706	1.2869	1.2640	1.2416	1.2196	1.1979

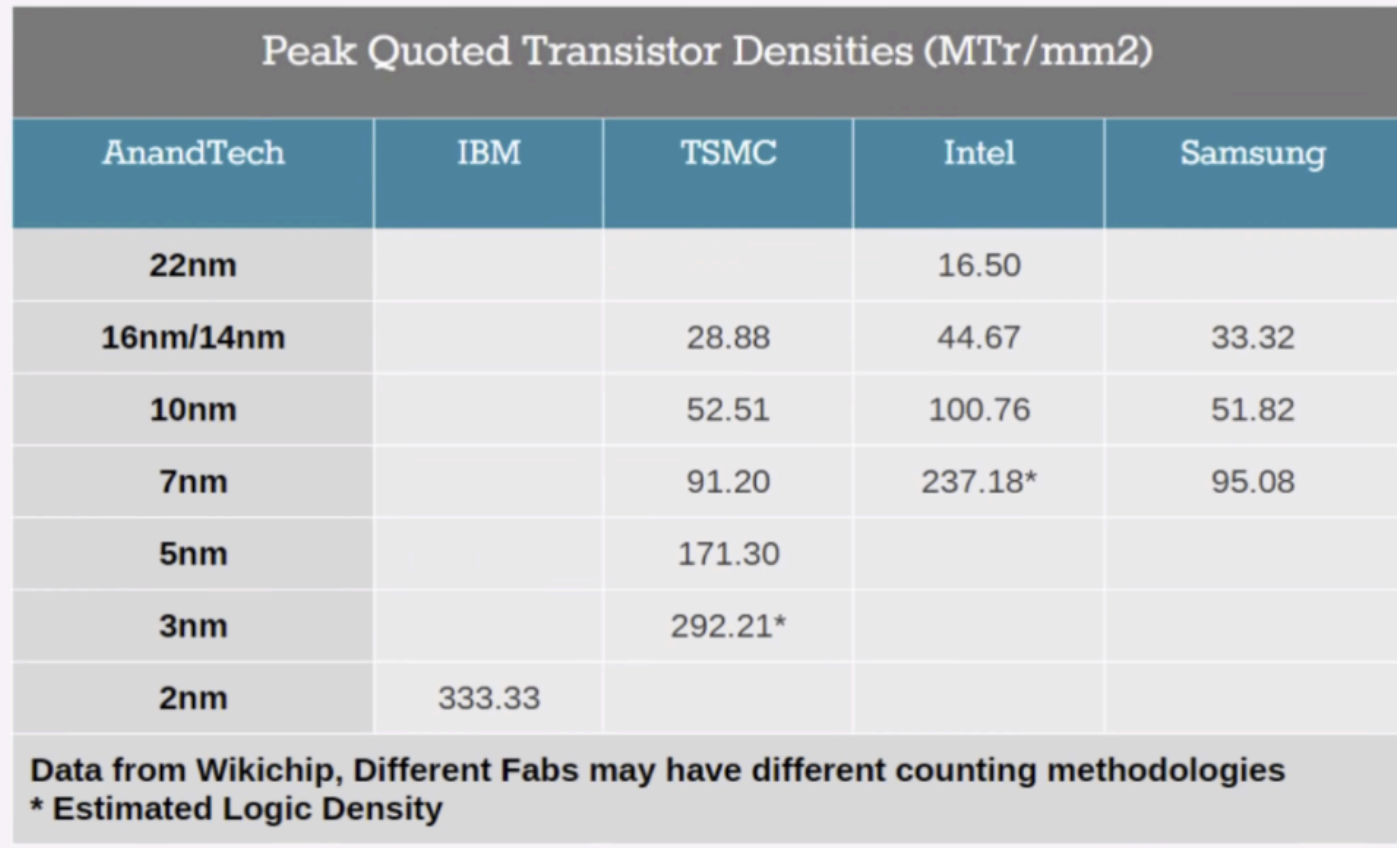
MPU = multiprocessor
ASIC = application-specific integrated circuit

2011 edition



Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
Logic Industry "Node Name" Label	**"16/14"**	**"10"**	**"7"**	**"5"**	**"3.5"**	**"2.5"**	**"1.8"**	
Logic ½ Pitch (nm)	**40**	**32**	**25**	**20**	**16**	**13**	**10**	**7**
Flash ½ Pitch [2D] (nm)	**18**	**15**	**13**	**11**	**9**	**8**	**8**	**8**
DRAM ½ Pitch (nm)	**28**	**24**	**20**	**17**	**14**	**12**	**10**	**7.7**
FinFET Fin Half-pitch (new) (nm)	**30**	**24**	**19**	**15**	**12**	**9.5**	**7.5**	**5.3**
FinFET Fin Width (new) (nm)	**7.6**	**7.2**	**6.8**	**6.4**	**6.1**	**5.7**	**5.4**	**5.0**
6-t SRAM Cell Size(um2) [@60f2]	**0.096**	**0.061**	**0.038**	**0.024**	**0.015**	**0.010**	**0.0060**	**0.0030**
MPU/ASIC HighPerf 4t NAND Gate Size(um2)	**0.248**	**0.157**	**0.099**	**0.062**	**0.039**	**0.025**	**0.018**	**0.009**
4-input NAND Gate Density (Kgates/mm) [@155f2]	**4.03E+03**	**6.37E+03**	**1.01E+04**	**1.61E+04**	**2.55E+04**	**4.05E+04**	**6.42E+04**	**1.28E+05**
Flash Generations Label (bits per chip) (SLC/MLC)	**64G /128G**	**128G /256G**	**256G / 512G**	**512G / 1T**	**512G / 1T**	**1T / 2T**	**2T / 4T**	**4T / 8T**
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	**16-32**	**16-32**	**16-32**	**32-64**	**48-96**	**64-128**	**96-192**	**192-384**
Flash 3D Layer half-pitch targets (nm)	**64nm**	**54nm**	**45nm**	**30nm**	**28nm**	**27nm**	**25nm**	**22nm**
DRAM Generations Label (bits per chip)	**4G**	**8G**	**8G**	**16G**	**32G**	**32G**	**32G**	**32G**
450mm Production High Volume Manufacturing Begins (100Kwspm)				**2018**				
Vdd (High Performance, high Vdd transistors)[**]	**0.86**	**0.83**	**0.80**	**0.77**	**0.74**	**0.71**	**0.68**	**0.64**
1/(CV/I) (1/psec) [**]	**1.13**	**1.53**	**1.75**	**1.97**	**2.10**	**2.29**	**2.52**	**3.17**
On-chip local clock MPU HP [at 4% CAGR]	**5.50**	**5.95**	**6.44**	**6.96**	**7.53**	**8.14**	**8.8**	**9.9**
Maximum number wiring levels [unchanged	**13**	**13**	**14**	**14**	**15**	**15**	**16**	**17**
MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	**28**	**22**	**18**	**14**	**11**	**9**	**7**	**5**
MPU High-Performance Physical Gate Length (GLph) (nm) [**]	**20**	**17**	**14**	**12**	**10**	**8**	**7**	**5**
ASIC/Low Standby Power (LP) Physical Gate Length (nm) (GLph)[**]	**23**	**19**	**16**	**13**	**11**	**9**	**8**	**6**

2013 edition

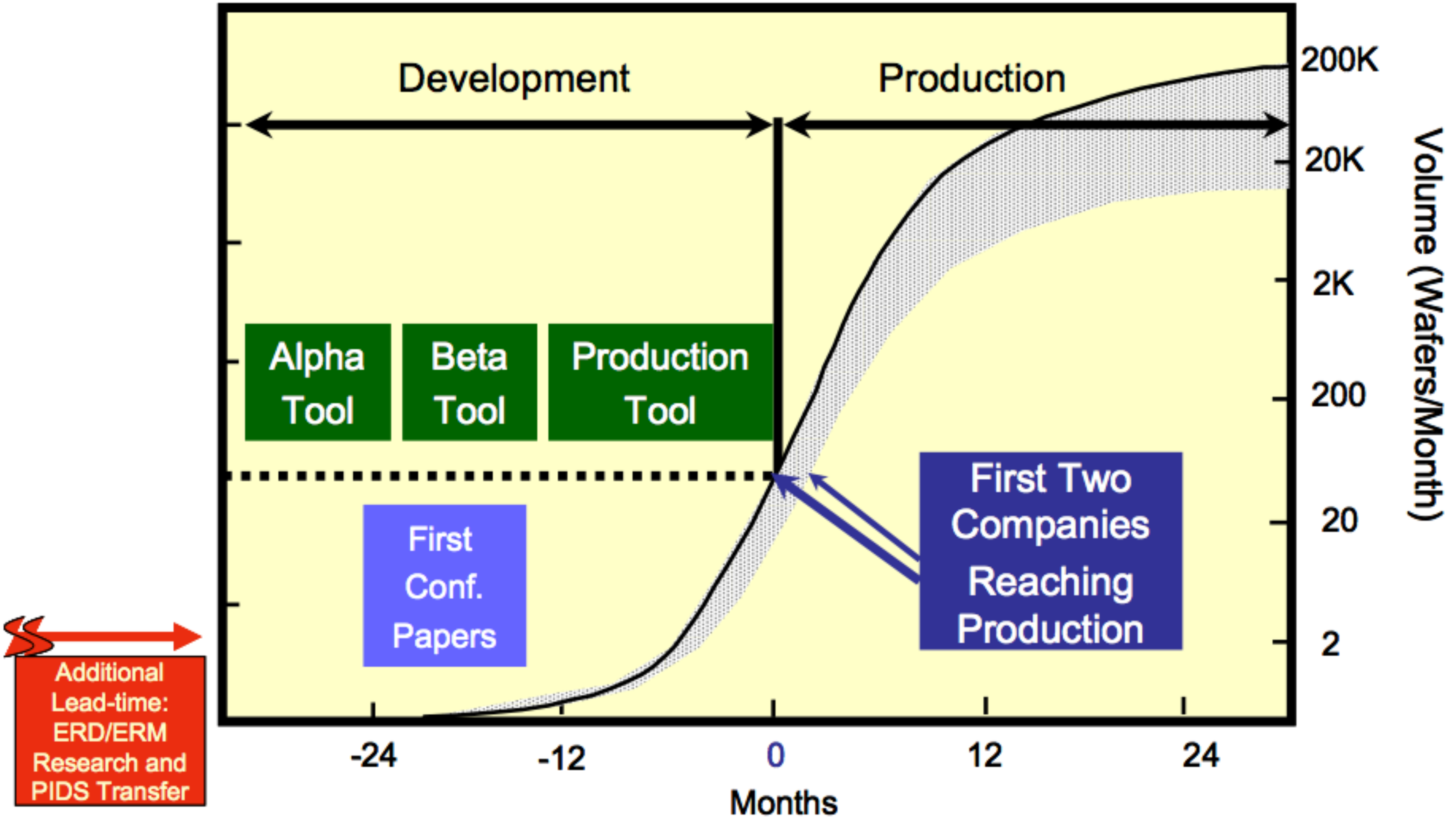


Peak Quoted Transistor Densities (MTr/mm2)

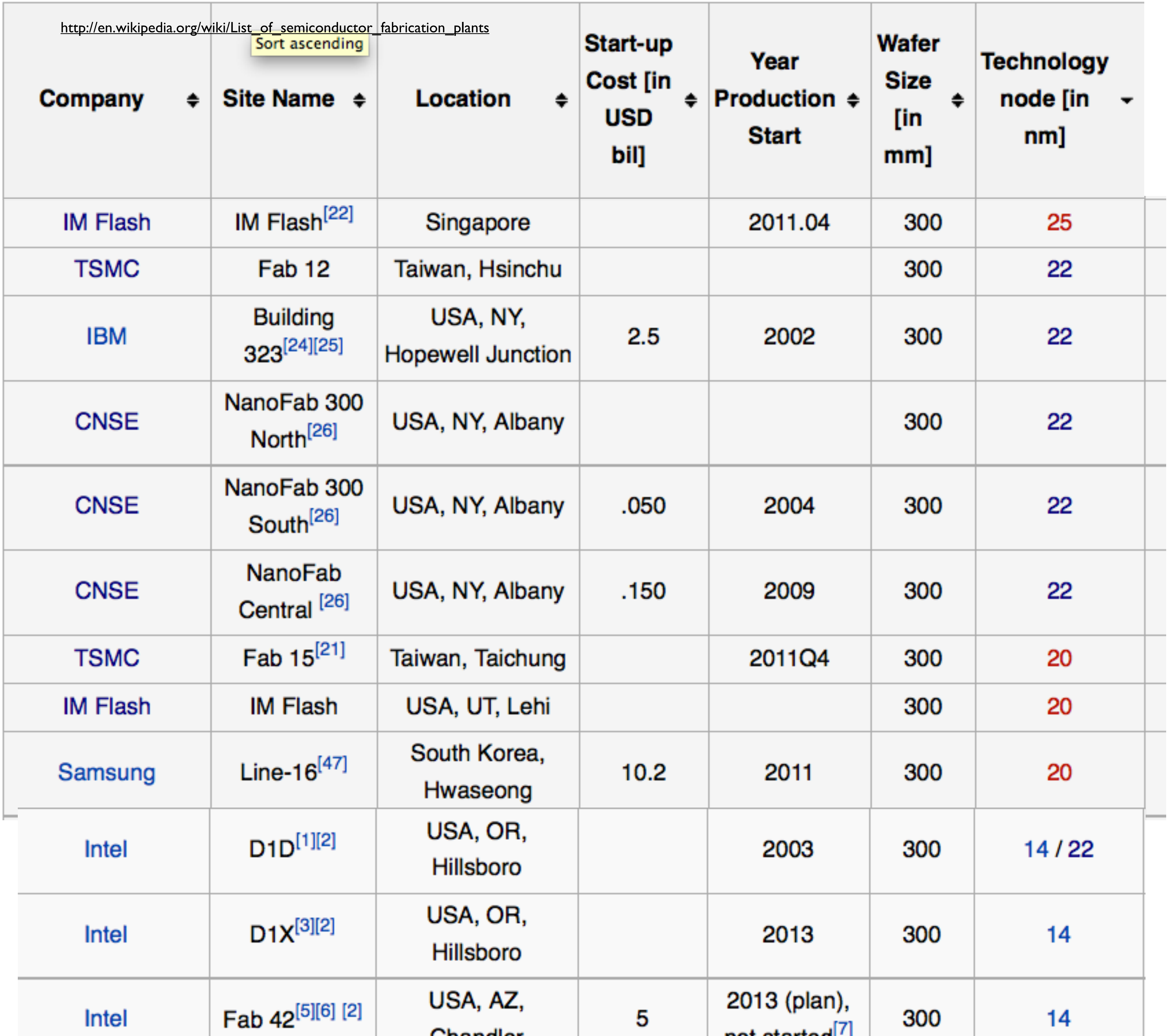
AnandTech	IBM	TSMC	Intel	Samsung
22nm			16.50	
16nm/14nm		28.88	44.67	33.32
10nm		52.51	100.76	51.82
7nm		91.20	237.18*	95.08
5nm		171.30		
3nm		292.21*		
2nm	333.33			

Data from Wikichip, Different Fabs may have different counting methodologies
*** Estimated Logic Density**

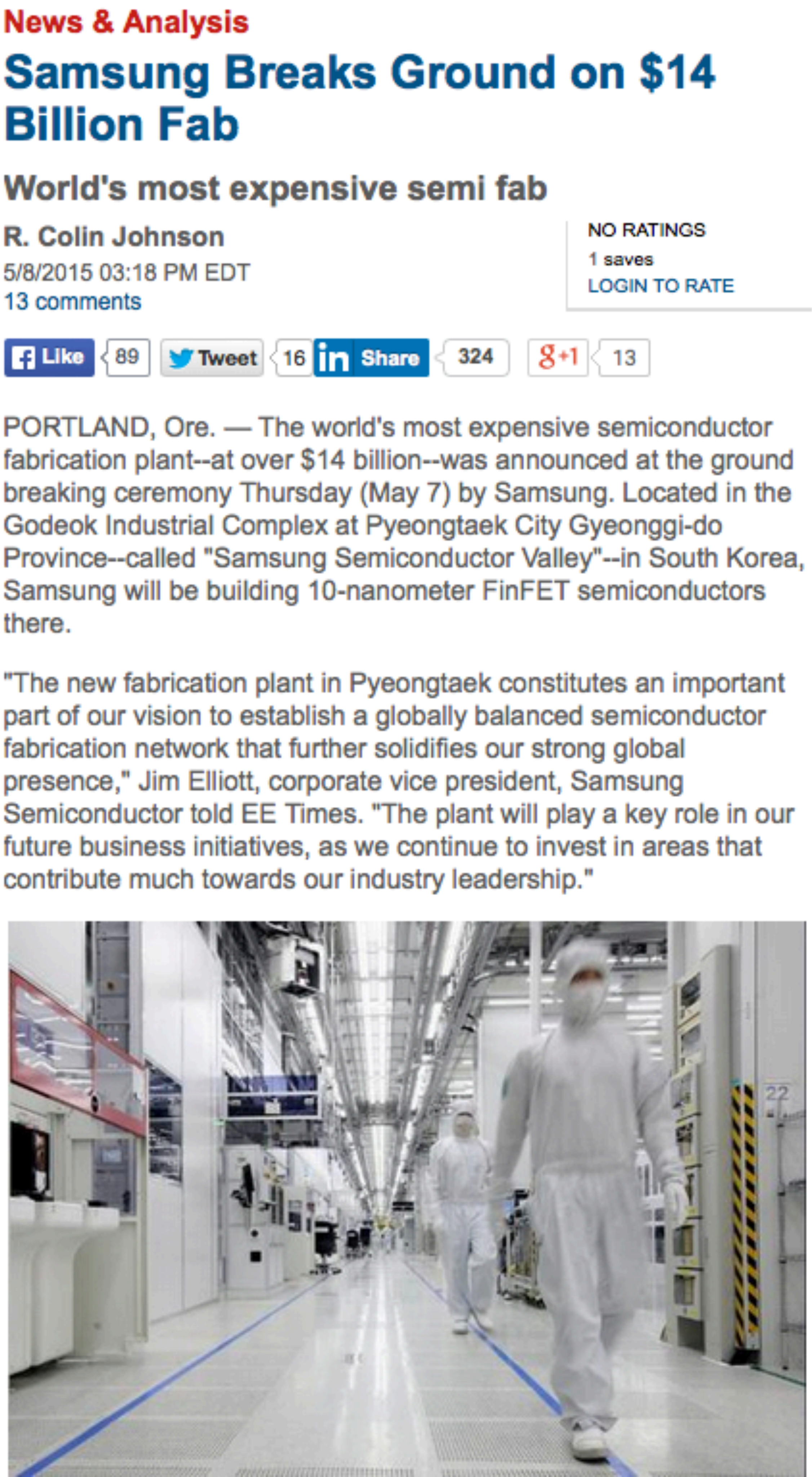
Production Ramp-up Model and Technology/Cycle Timing



http://en.wikipedia.org/wiki/List_of_semiconductor_fabrication_plants



Company	Site Name	Location	Start-up Cost [in USD bil]	Year Production Start	Wafer Size [in mm]	Technology node [in nm]
IM Flash	IM Flash[22]	Singapore		2011.04	300	25
TSMC	Fab 12	Taiwan, Hsinchu			300	22
IBM	Building 323[24][25]	USA, NY, Hopewell Junction	2.5	2002	300	22
CNSE	NanoFab 300 North[26]	USA, NY, Albany			300	22
CNSE	NanoFab 300 South[26]	USA, NY, Albany	.050	2004	300	22
CNSE	NanoFab Central [26]	USA, NY, Albany	.150	2009	300	22
TSMC	Fab 15[21]	Taiwan, Taichung		2011Q4	300	20
IM Flash	IM Flash	USA, UT, Lehi			300	20
Samsung	Line-16[47]	South Korea, Hwaseong	10.2	2011	300	20
Intel	D1D[1][2]	USA, OR, Hillsboro		2003	300	14 / 22
Intel	D1X[3][2]	USA, OR, Hillsboro		2013	300	14
Intel	Fab 42[5][6] [2]	USA, AZ, Chandler	5	2013 (plan), not started[7]	300	14



News & Analysis

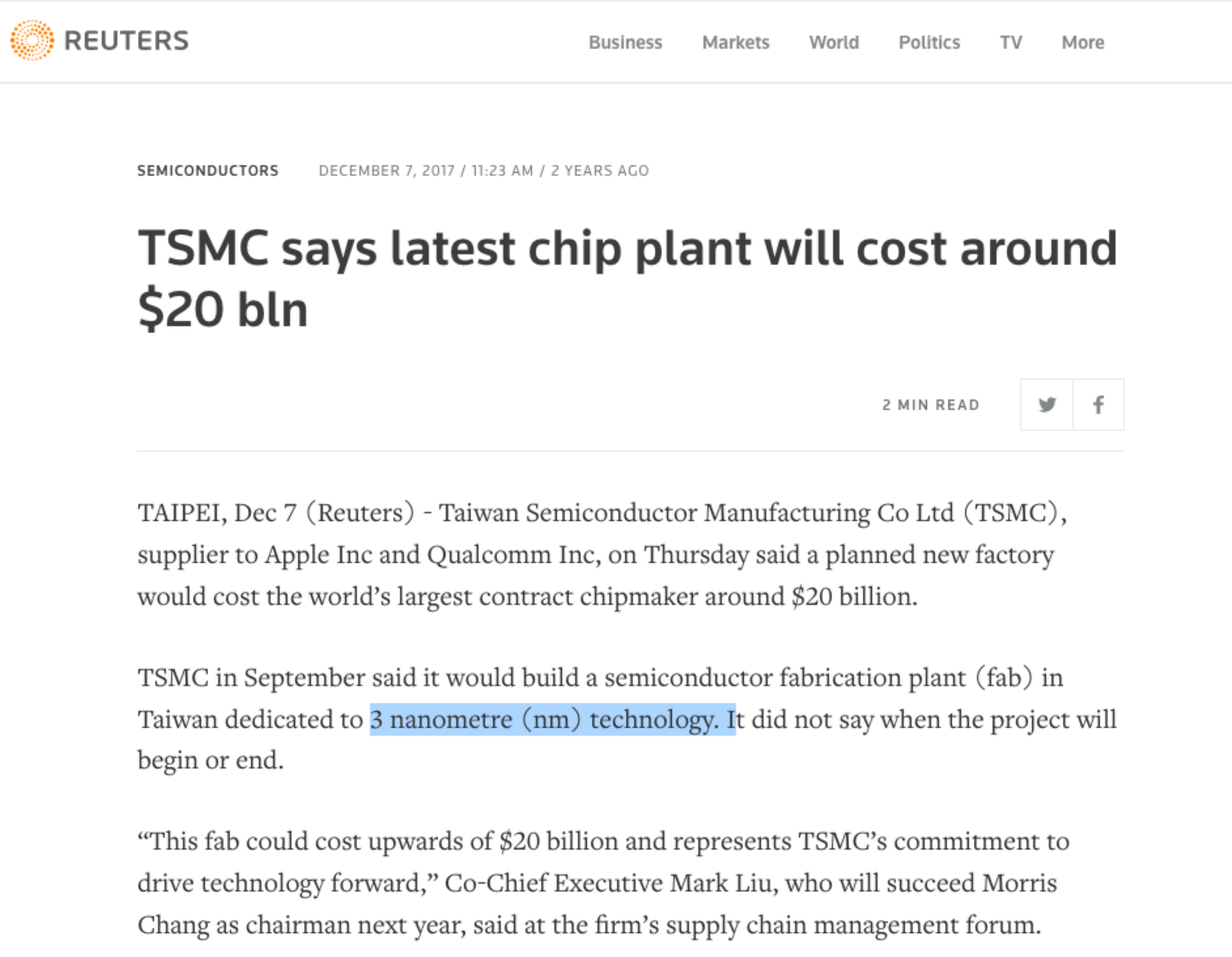
Samsung Breaks Ground on $14 Billion Fab

World's most expensive semi fab

R. Colin Johnson
5/8/2015 03:18 PM EDT
13 comments

PORTLAND, Ore. — The world's most expensive semiconductor fabrication plant--at over $14 billion--was announced at the ground breaking ceremony Thursday (May 7) by Samsung. Located in the Godeok Industrial Complex at Pyeongtaek City Gyeonggi-do Province--called "Samsung Semiconductor Valley"--in South Korea, Samsung will be building 10-nanometer FinFET semiconductors there.

"The new fabrication plant in Pyeongtaek constitutes an important part of our vision to establish a globally balanced semiconductor fabrication network that further solidifies our strong global presence," Jim Elliott, corporate vice president, Samsung Semiconductor told EE Times. "The plant will play a key role in our future business initiatives, as we continue to invest in areas that contribute much towards our industry leadership."



SEMICONDUCTORS DECEMBER 7, 2017 / 11:23 AM / 2 YEARS AGO

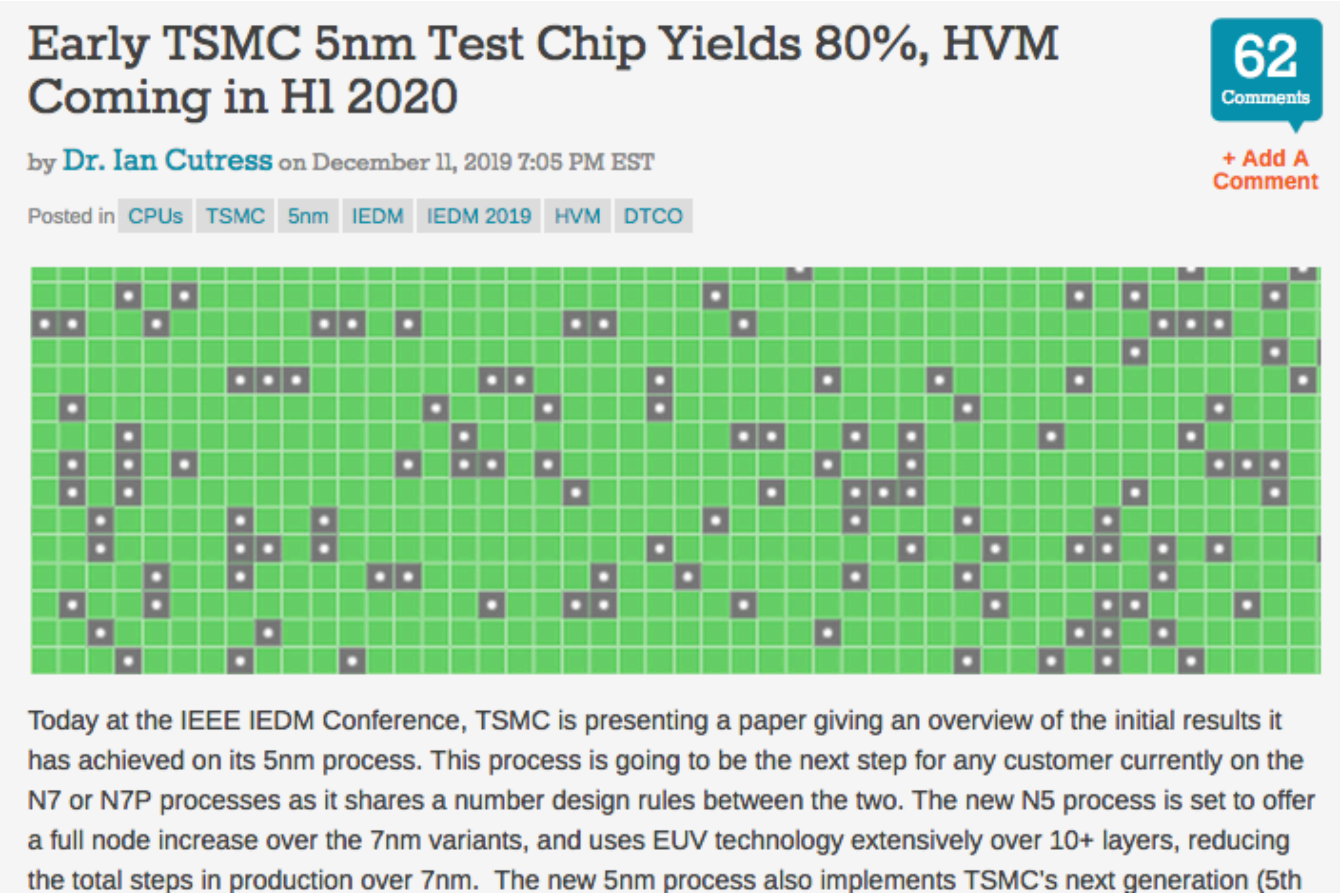
TSMC says latest chip plant will cost around $20 bln

TAIPEI, Dec 7 (Reuters) - Taiwan Semiconductor Manufacturing Co Ltd (TSMC), supplier to Apple Inc and Qualcomm Inc, on Thursday said a planned new factory would cost the world's largest contract chipmaker around $20 billion.

TSMC in September said it would build a semiconductor fabrication plant (fab) in Taiwan dedicated to 3 nanometre (nm) technology. It did not say when the project will begin or end.

"This fab could cost upwards of $20 billion and represents TSMC's commitment to drive technology forward," Co-Chief Executive Mark Liu, who will succeed Morris Chang as chairman next year, said at the firm's supply chain management forum.

https://www.anandtech.com/show/15219/early-tsmc-5nm-test-chip-yields-80-hvm-coming-in-h1-2020

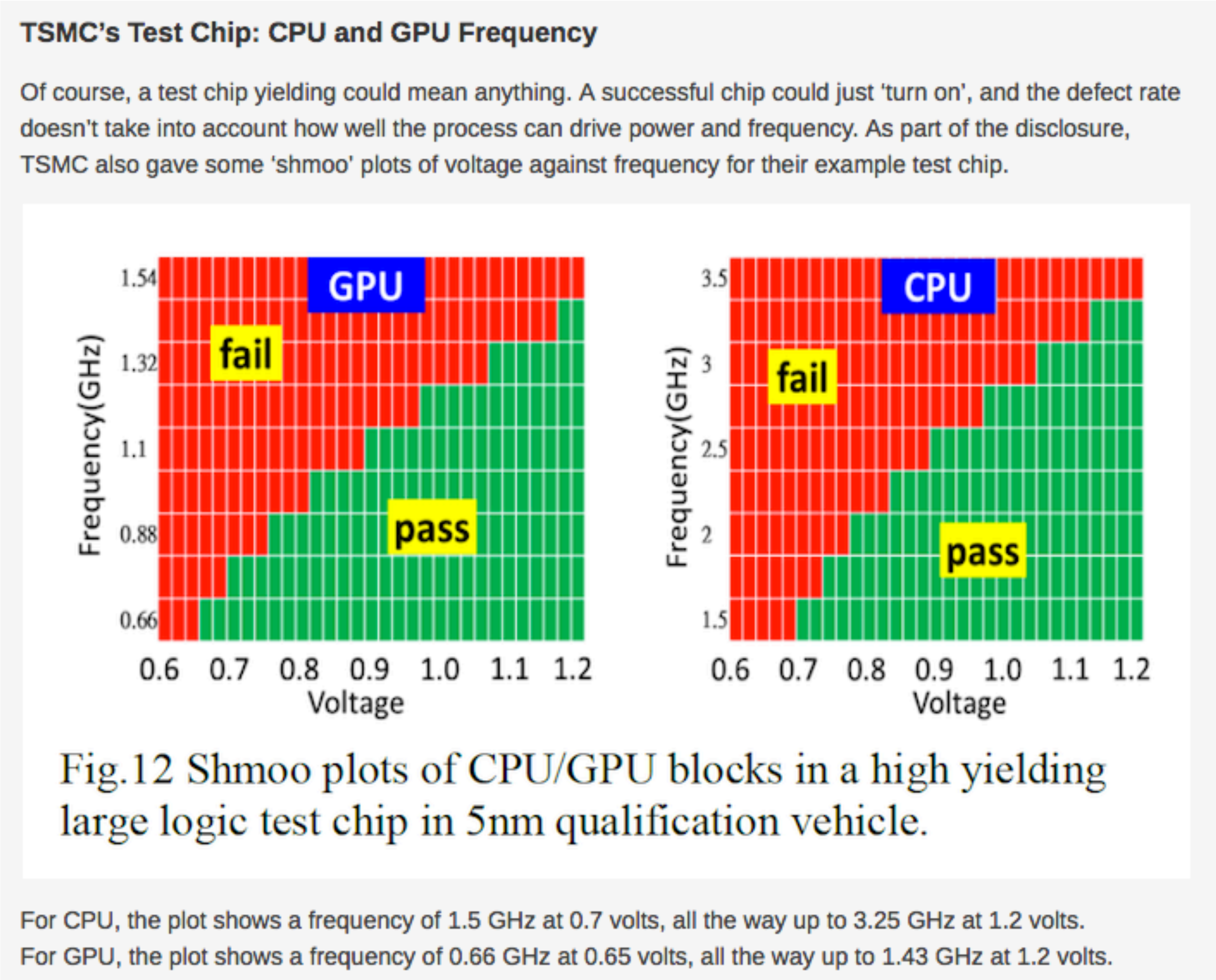


Early TSMC 5nm Test Chip Yields 80%, HVM Coming in H1 2020

by **Dr. Ian Cutress** on December 11, 2019 7:05 PM EST

Posted in CPUs TSMC 5nm IEDM IEDM 2019 HVM DTCO

Today at the IEEE IEDM Conference, TSMC is presenting a paper giving an overview of the initial results it has achieved on its 5nm process. This process is going to be the next step for any customer currently on the N7 or N7P processes as it shares a number design rules between the two. The new N5 process is set to offer a full node increase over the 7nm variants, and uses EUV technology extensively over 10+ layers, reducing the total steps in production over 7nm. The new 5nm process also implements TSMC's next generation (5th



TSMC’s Test Chip: CPU and GPU Frequency

Of course, a test chip yielding could mean anything. A successful chip could just ‘turn on’, and the defect rate doesn’t take into account how well the process can drive power and frequency. As part of the disclosure, TSMC also gave some ‘shmoo’ plots of voltage against frequency for their example test chip.

Fig.12 Shmoo plots of CPU/GPU blocks in a high yielding large logic test chip in 5nm qualification vehicle.

For CPU, the plot shows a frequency of 1.5 GHz at 0.7 volts, all the way up to 3.25 GHz at 1.2 volts.
For GPU, the plot shows a frequency of 0.66 GHz at 0.65 volts, all the way up to 1.43 GHz at 1.2 volts.

IO Demonstration: PAM4

One of the key elements in future chips is the ability to support multiple communication technologies, and in the test chip TSMC also included a transceiver designed to enable high-speed PAM-4.

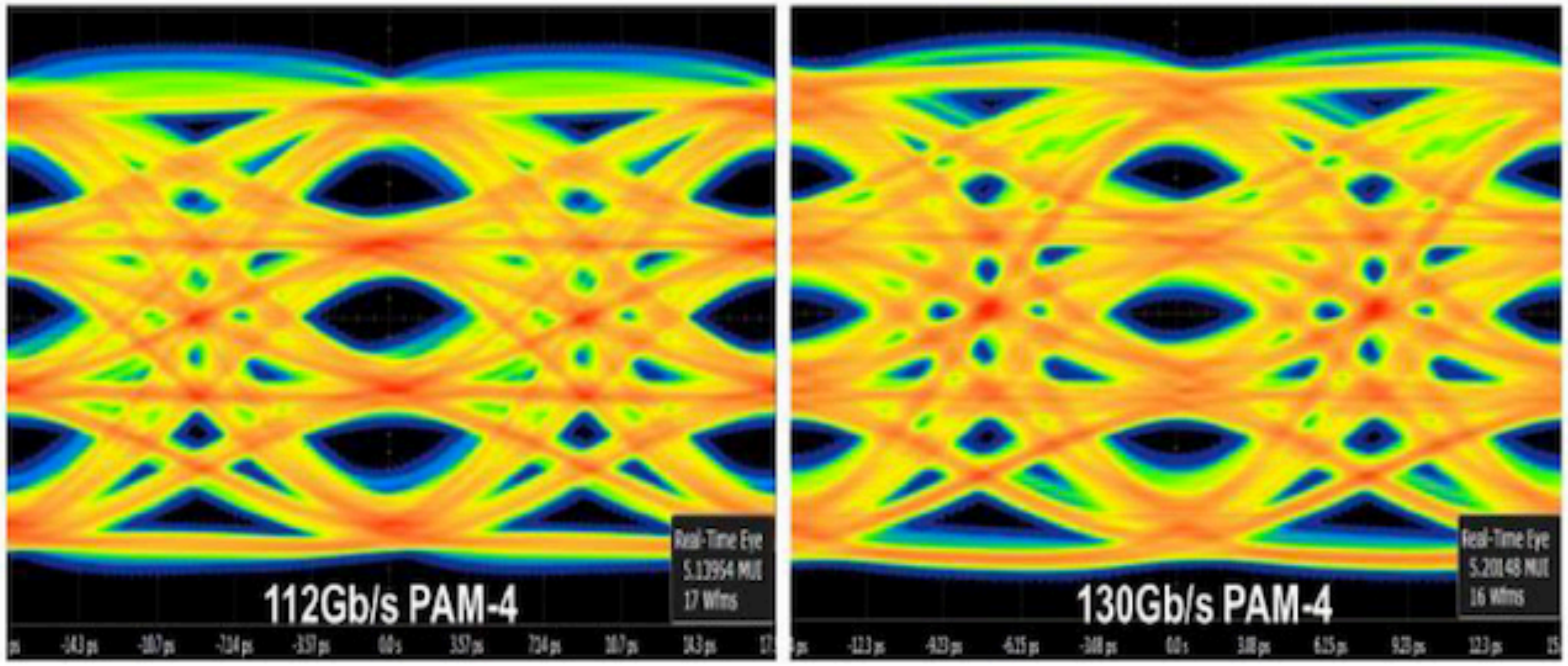
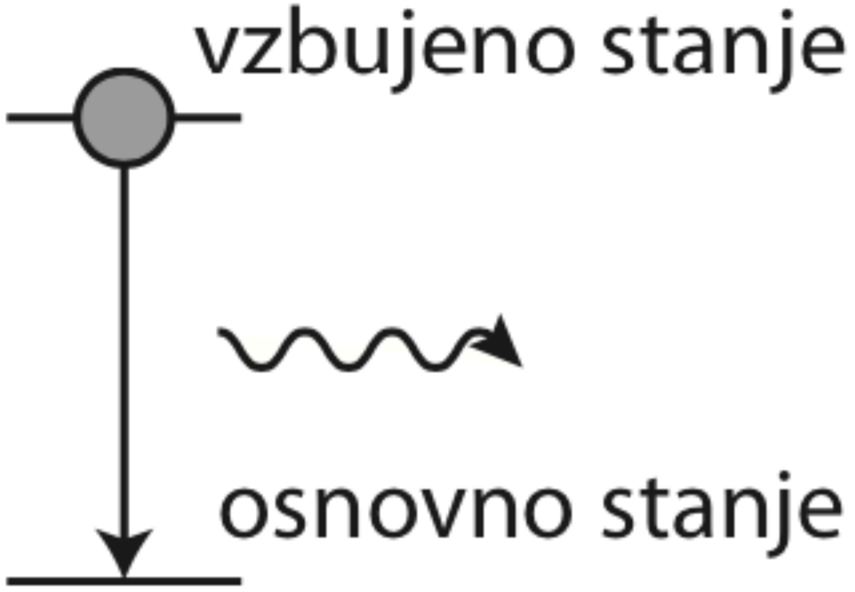


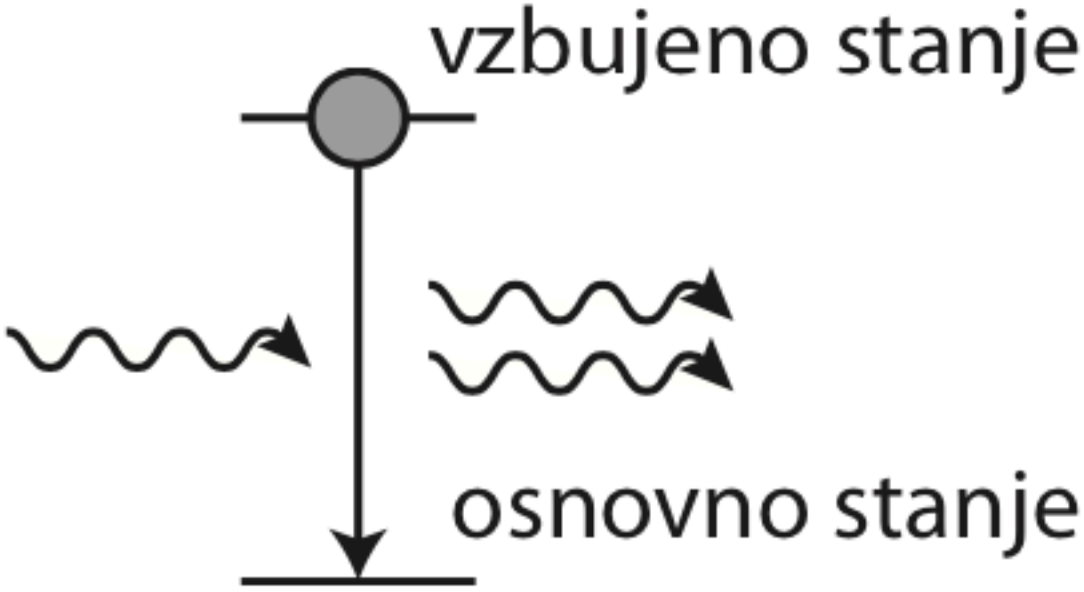
Fig.16 High speed PAM-4 transmitters build in a 5nm test chip demonstrate highest speed of 130Gb/s with 0.96pJ/bit and nominal 112Gb/s with 0.78pJ/bit energy efficiency [5]

We have already seen 112 Gb/s transceivers on other processes, and TSMC was able to do 112 Gb/s here with a 0.76 pJ/bit energy efficiency. Pushing the bandwidth further, TSMC was able to get 130 Gb/s still within tolerances in the eye diagram, but at a 0.96 pJ/bit efficiency. This bodes well for any PAM-4 based technologies, such as PCIe 6.0.

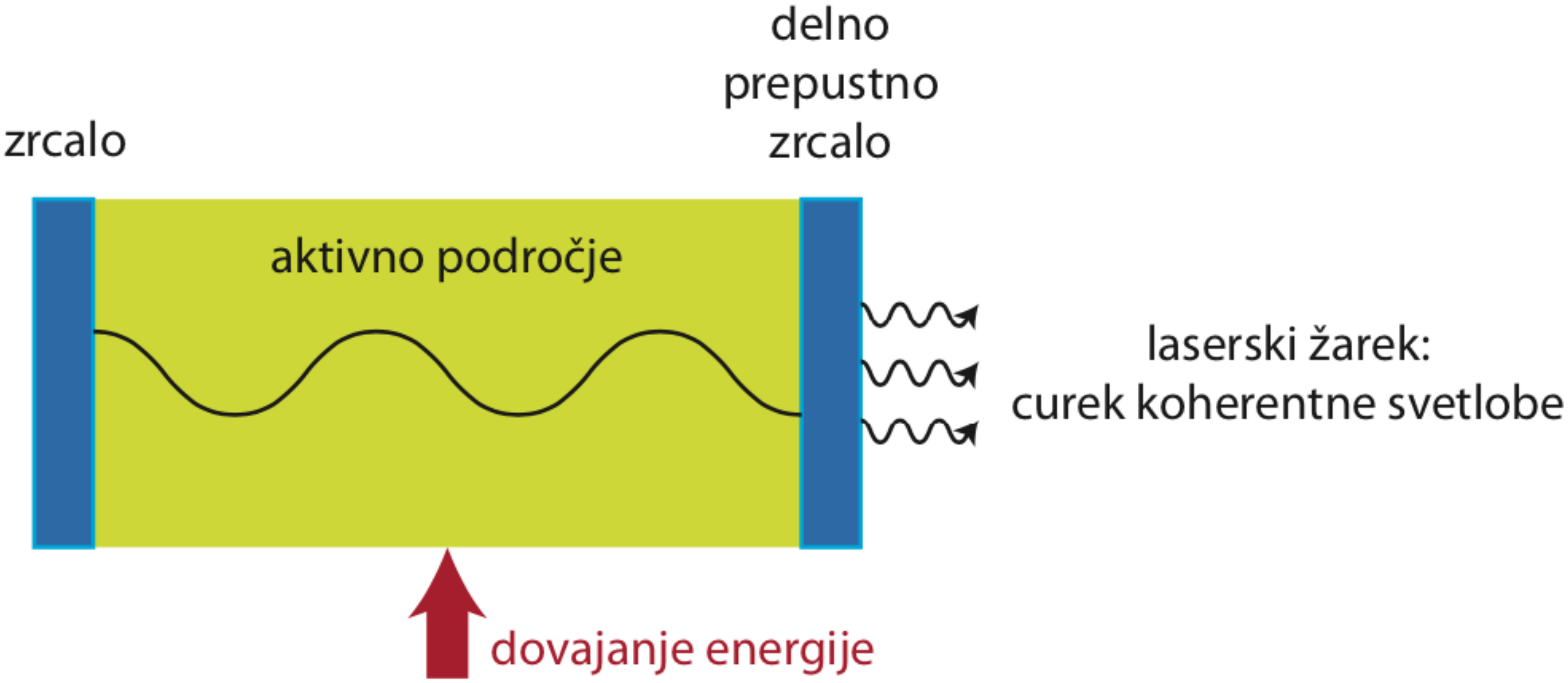
Kaj je laser?
Kako se razlikujeta spontano in stimulirano sevanje?



spontano sevanje



stimulirano sevanje



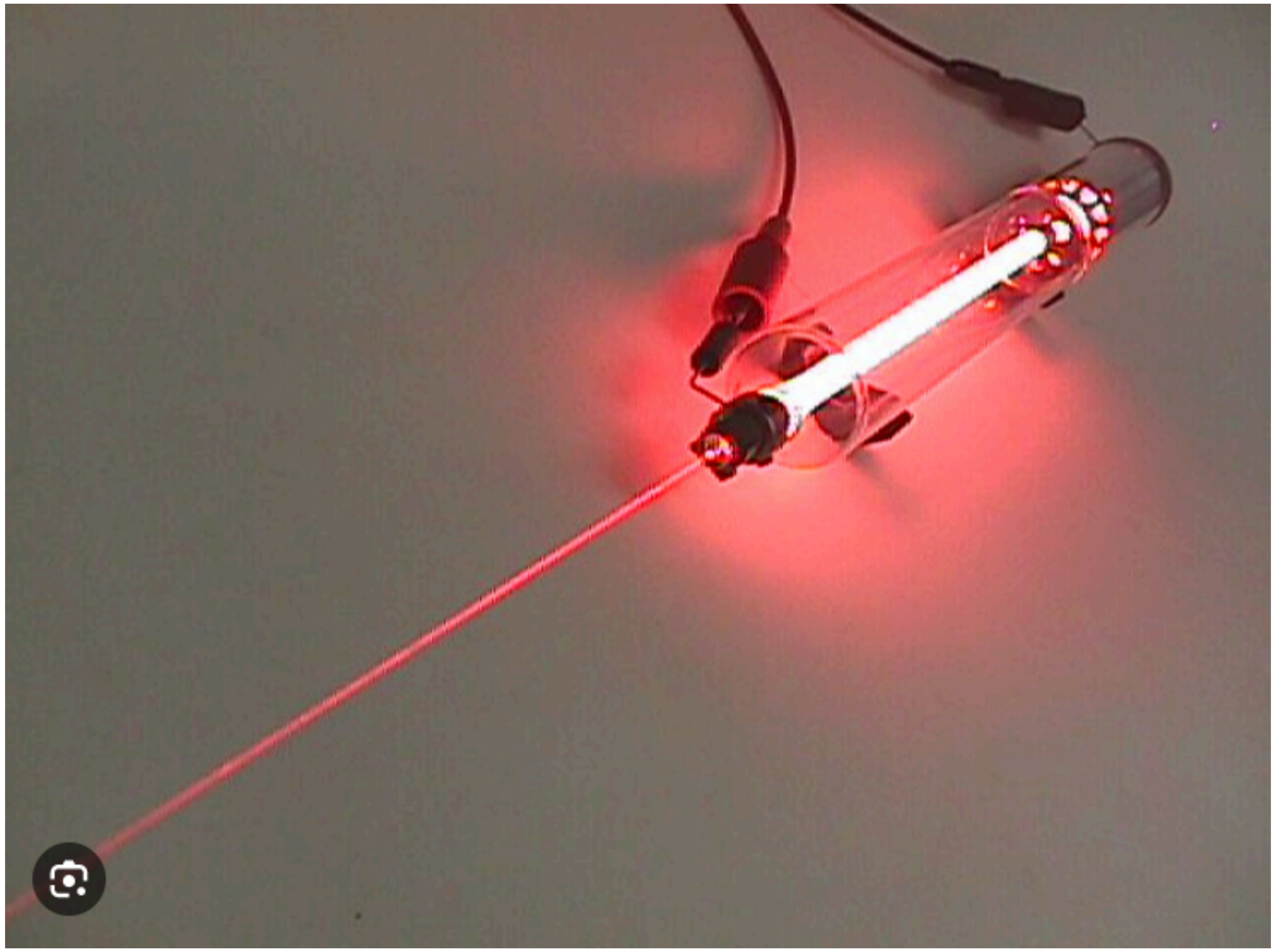
zrcalo

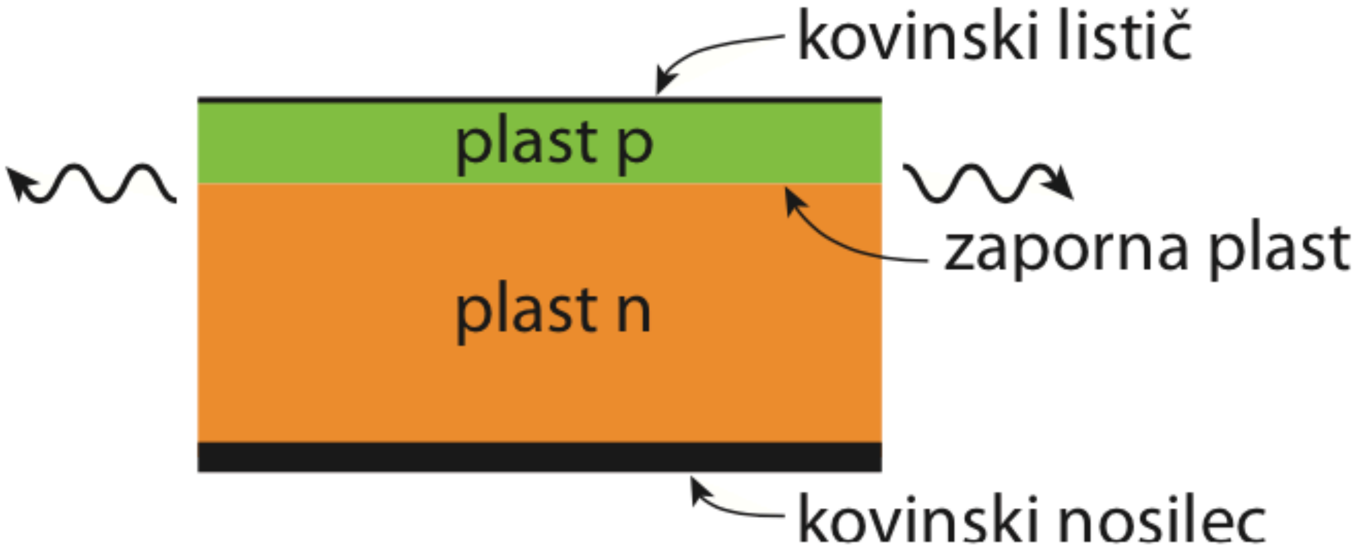
delno
prepustno
zrcalo

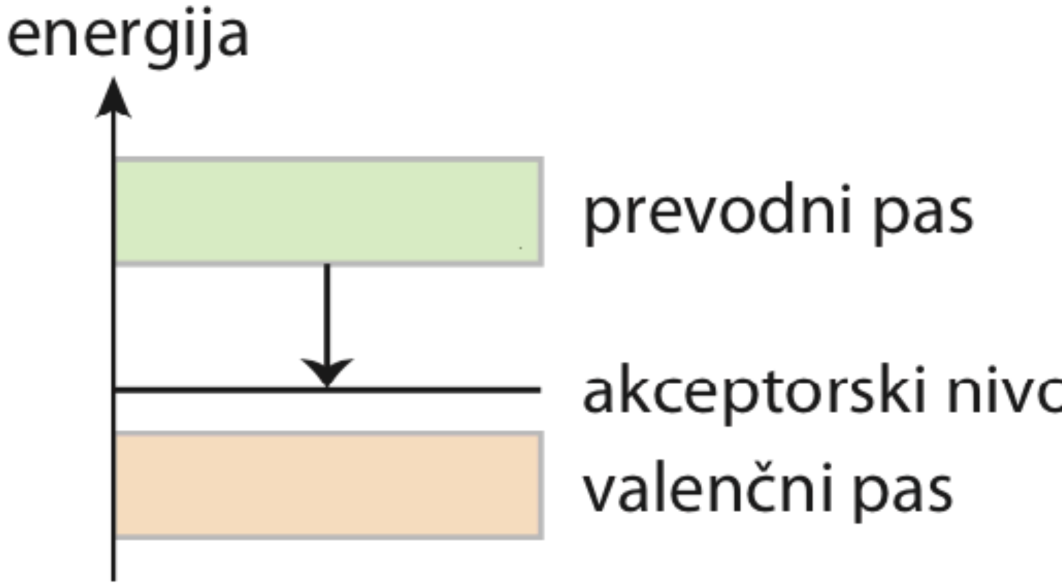
aktivno področje

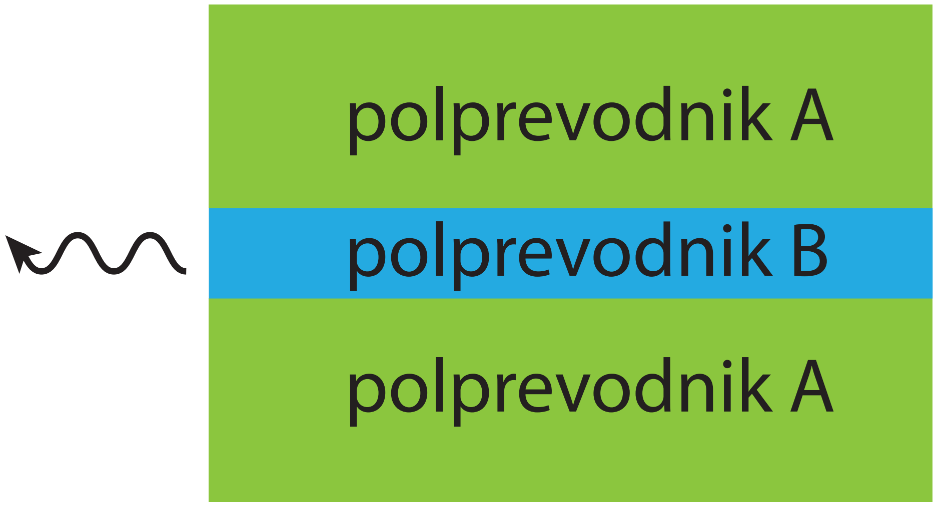
laserski žarek:
curek koherentne svetlobe

dovajanje energije




kovinski listič
plast p
zaporna plast
plast n
kovinski nosilec

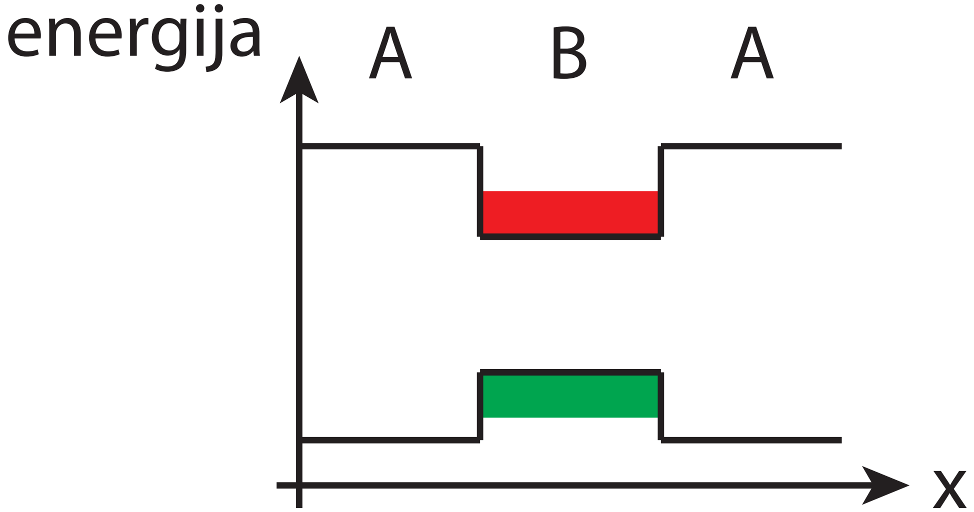

energija
prevodni pas
akceptorski nivo
valenčni pas

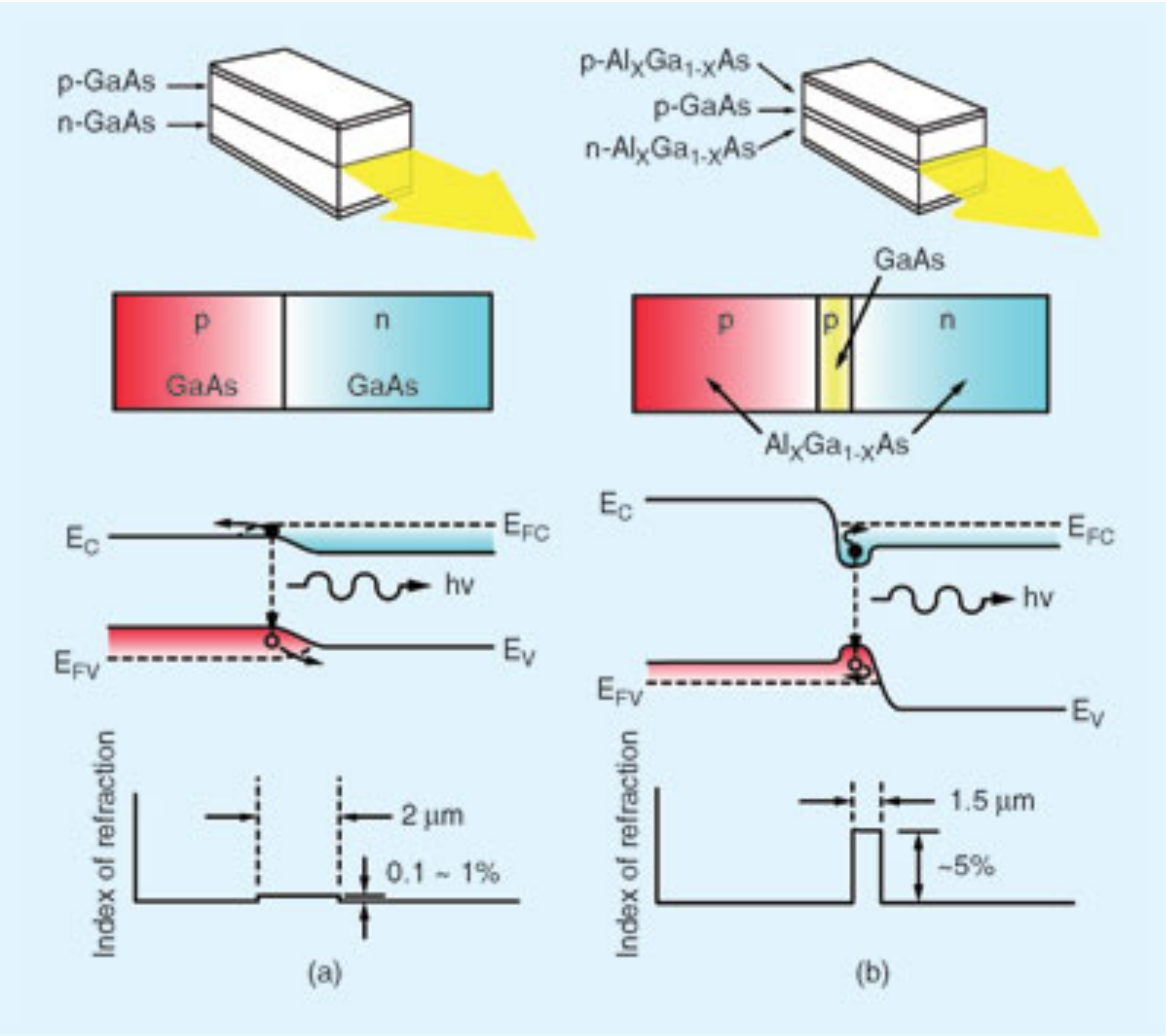


polprevodnik A

polprevodnik B

polprevodnik A





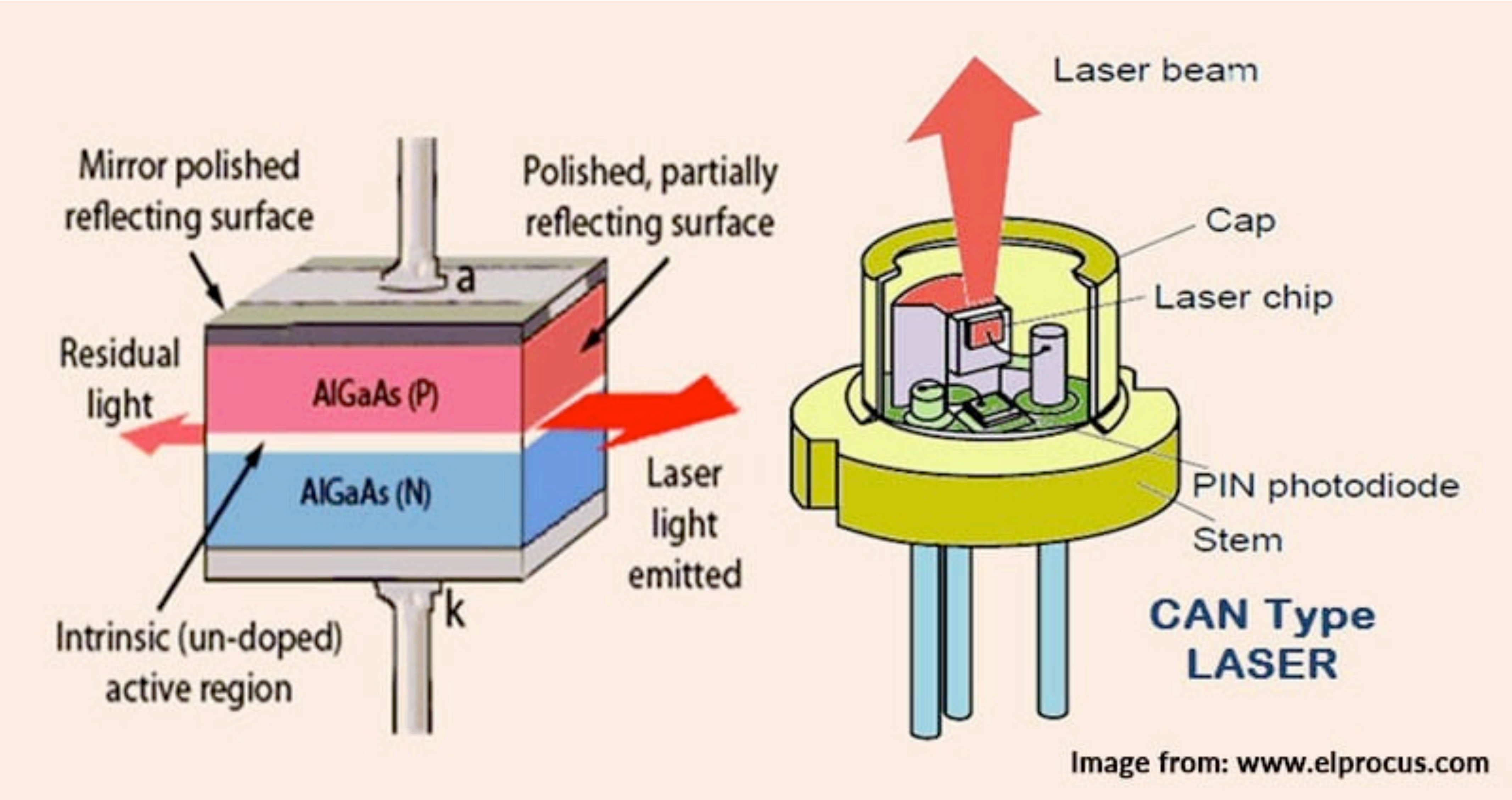


Image from: www.elprocus.com

Products Home / Lasers / Coherent Sources / Laser Diodes by Wavelength

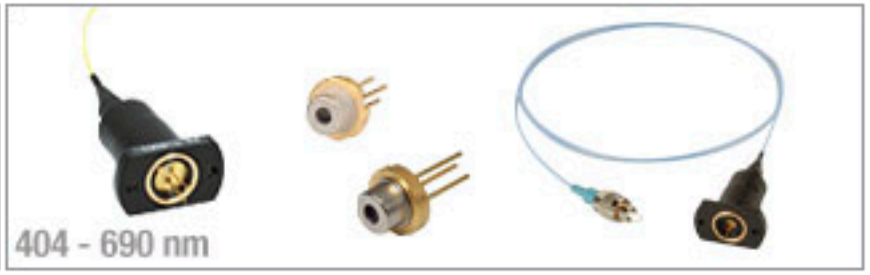
Laser Diodes by Wavelength

Laser diodes, which are capable of converting electrical current into light, are available from Thorlabs with center wavelengths in the 375 - 2000 nm range and output powers from 1.5 mW up to 3 W. We also offer Quantum Cascade Lasers (QCLs) with center wavelengths ranging from 4.05 to 11.00 µm. Our semiconductor laser diodes come in a variety of packages, including standard Ø5.6 mm and Ø9 mm TO-cans, butterfly, laser pigtail, and chip on submount. QCLs come in Ø9 mm, C-mount, D-mount, and high heat load packages. We also offer optoelectronics mounts that directly accommodate many of our laser diode package options.

The Laser Diode Selection Guide provides a comprehensive list of all laser diodes available from stock, along with key specifications.

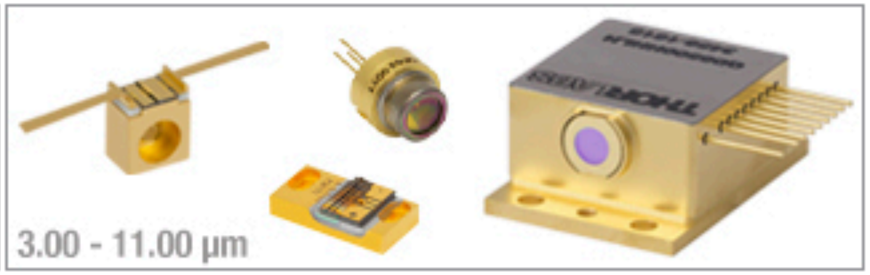
UV Laser Diode

Visible Laser Diodes



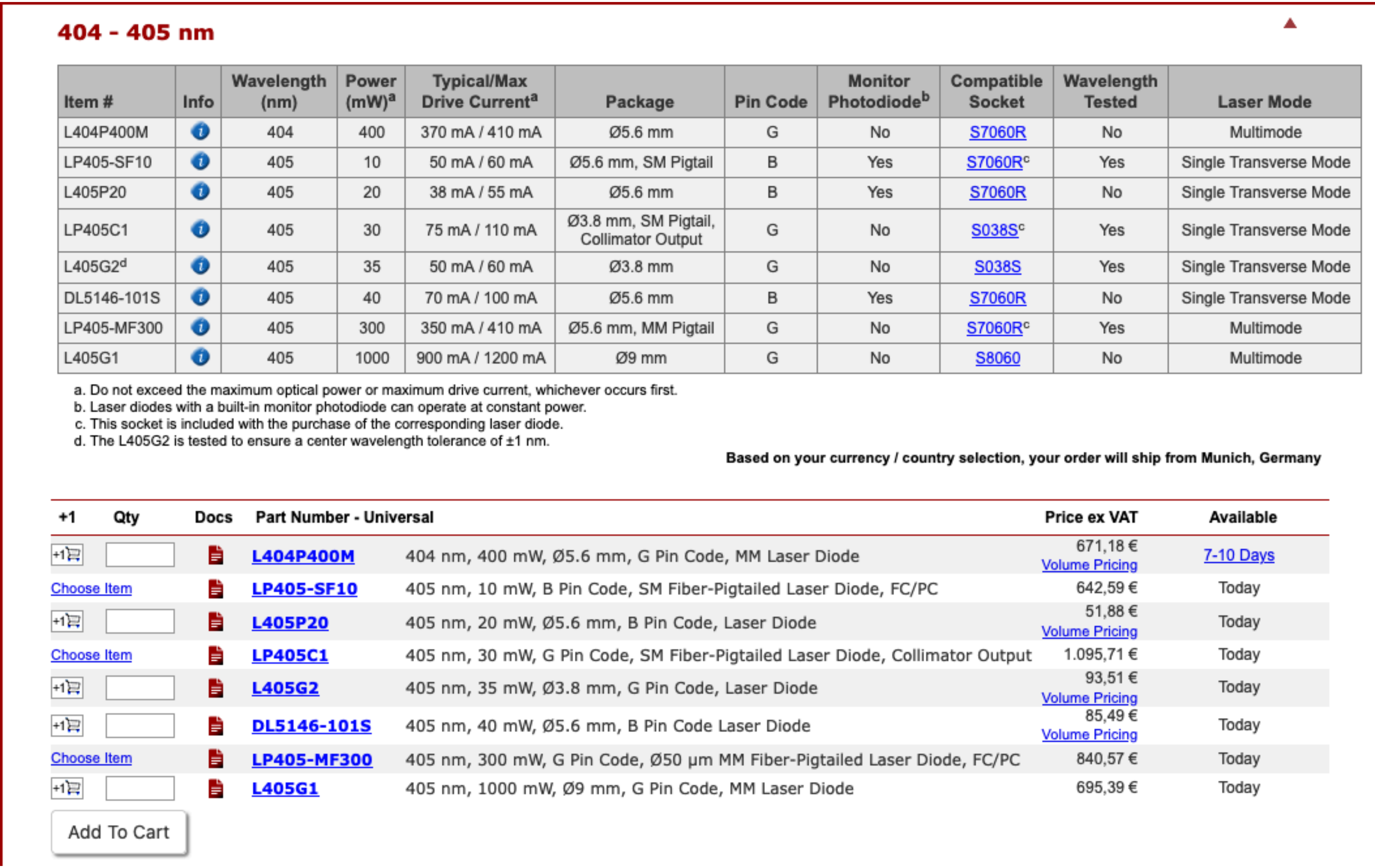
NIR Laser Diodes

MIR Quantum Cascade Lasers



Optoelectronic Mounts for Laser Diodes

Laser Diode Selection Guide



404 - 405 nm

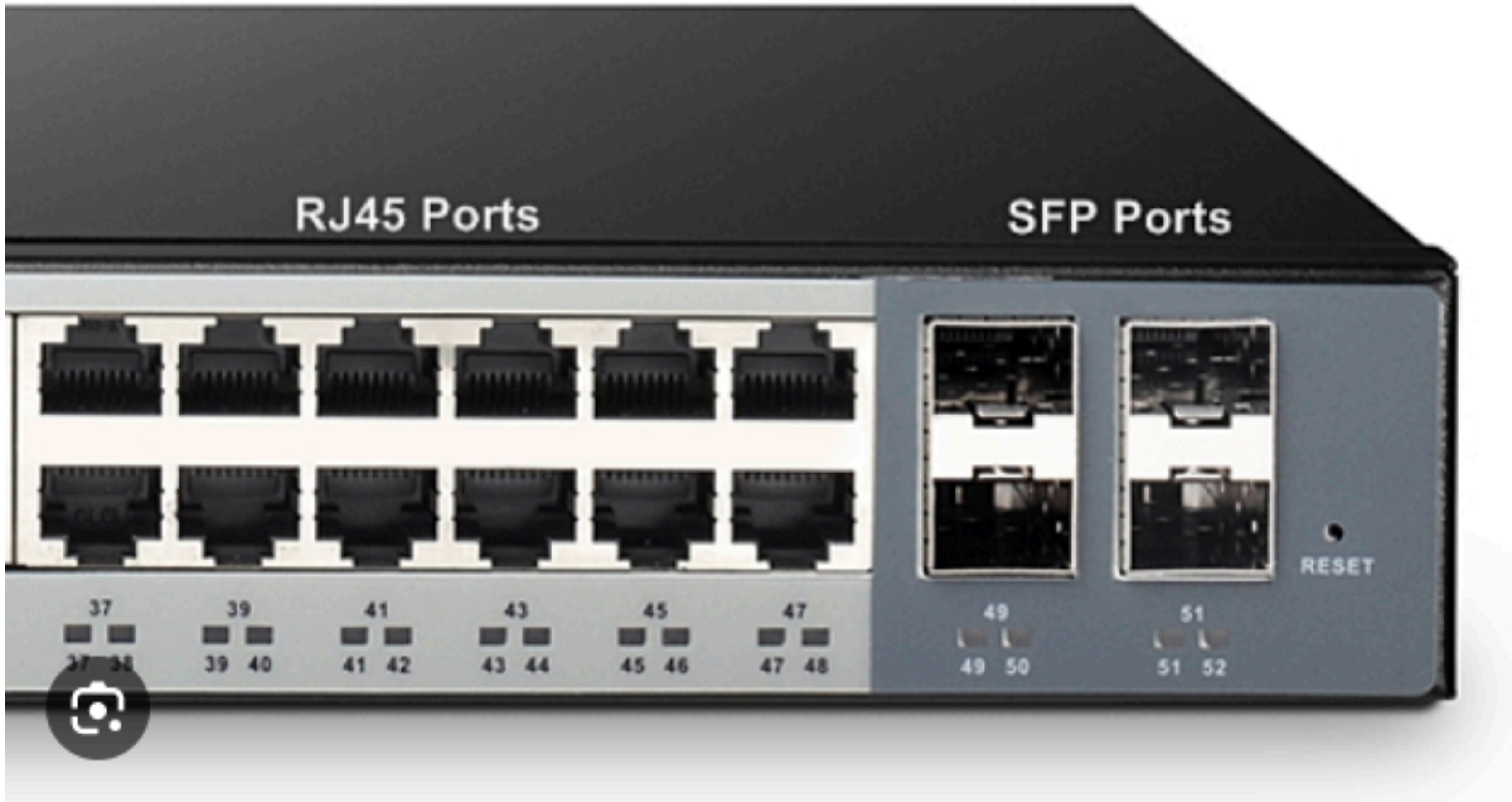
Item #	Info	Wavelength (nm)	Power (mW)[a]	Typical/Max Drive Current[a]	Package	Pin Code	Monitor Photodiode[b]	Compatible Socket	Wavelength Tested	Laser Mode
L404P400M	ⓘ	404	400	370 mA / 410 mA	Ø5.6 mm	G	No	S7060R	No	Multimode
LP405-SF10	ⓘ	405	10	50 mA / 60 mA	Ø5.6 mm, SM Pigtail	B	Yes	S7060R[c]	Yes	Single Transverse Mode
L405P20	ⓘ	405	20	38 mA / 55 mA	Ø5.6 mm	B	Yes	S7060R	No	Single Transverse Mode
LP405C1	ⓘ	405	30	75 mA / 110 mA	Ø3.8 mm, SM Pigtail, Collimator Output	G	No	S038S[c]	Yes	Single Transverse Mode
L405G2[d]	ⓘ	405	35	50 mA / 60 mA	Ø3.8 mm	G	No	S038S	Yes	Single Transverse Mode
DL5146-101S	ⓘ	405	40	70 mA / 100 mA	Ø5.6 mm	B	Yes	S7060R	No	Single Transverse Mode
LP405-MF300	ⓘ	405	300	350 mA / 410 mA	Ø5.6 mm, MM Pigtail	G	No	S7060R[c]	Yes	Multimode
L405G1	ⓘ	405	1000	900 mA / 1200 mA	Ø9 mm	G	No	S8060	No	Multimode

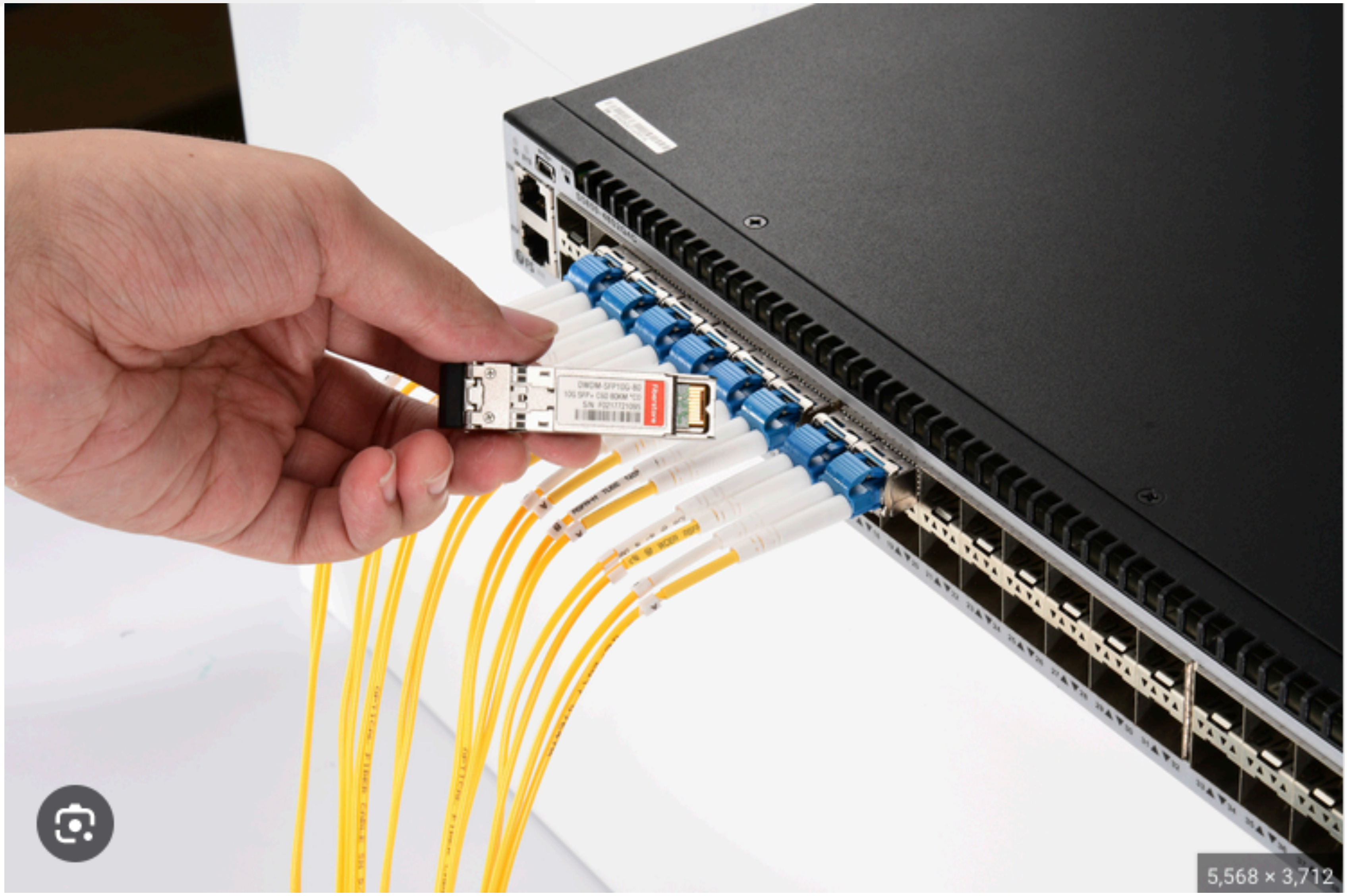
a. Do not exceed the maximum optical power or maximum drive current, whichever occurs first.
b. Laser diodes with a built-in monitor photodiode can operate at constant power.
c. This socket is included with the purchase of the corresponding laser diode.
d. The L405G2 is tested to ensure a center wavelength tolerance of ±1 nm.

Based on your currency / country selection, your order will ship from Munich, Germany

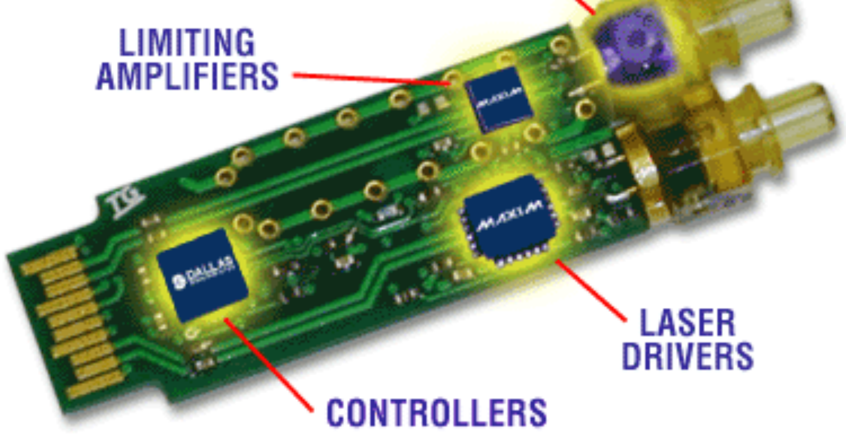
+1	Qty	Docs	Part Number - Universal		Price ex VAT	Available
+1			**L404P400M**	404 nm, 400 mW, Ø5.6 mm, G Pin Code, MM Laser Diode	671,18 € Volume Pricing	7-10 Days
Choose Item			**LP405-SF10**	405 nm, 10 mW, B Pin Code, SM Fiber-Pigtailed Laser Diode, FC/PC	642,59 €	Today
+1			**L405P20**	405 nm, 20 mW, Ø5.6 mm, B Pin Code, Laser Diode	51,88 € Volume Pricing	Today
Choose Item			**LP405C1**	405 nm, 30 mW, G Pin Code, SM Fiber-Pigtailed Laser Diode, Collimator Output	1.095,71 €	Today
+1			**L405G2**	405 nm, 35 mW, Ø3.8 mm, G Pin Code, Laser Diode	93,51 € Volume Pricing	Today
+1			**DL5146-101S**	405 nm, 40 mW, Ø5.6 mm, B Pin Code Laser Diode	85,49 € Volume Pricing	Today
Choose Item			**LP405-MF300**	405 nm, 300 mW, G Pin Code, Ø50 µm MM Fiber-Pigtailed Laser Diode, FC/PC	840,57 €	Today
+1			**L405G1**	405 nm, 1000 mW, Ø9 mm, G Pin Code, MM Laser Diode	695,39 €	Today

Add To Cart


RJ45 Ports
SFP Ports
37
39
41
43
45
47
49
51
37 38
39 40
41 42
43 44
45 46
47 48
49 50
51 52
RESET


5,568 × 3,712


DIAMOND
CT-1250NSP-SB1L-D F3
CT-1250NSP-SB1L-D F3


TRANSIMPEDANCE AMPLIFIERS
LIMITING AMPLIFIERS
MAXIM
DALLAS
LASER DRIVERS
CONTROLLERS

The Nobel Prize in Physics 2009
Charles K. Kao, Willard S. Boyle, George E. Smith

Share this: 46

Charles K. Kao - Facts

Photo: U. Montan

Charles Kuen Kao

Born: 4 November 1933, Shanghai, China

Affiliation at the time of the award: Standard Telecommunication Laboratories, Harlow, United Kingdom, Chinese University of Hong Kong, Hong Kong, China

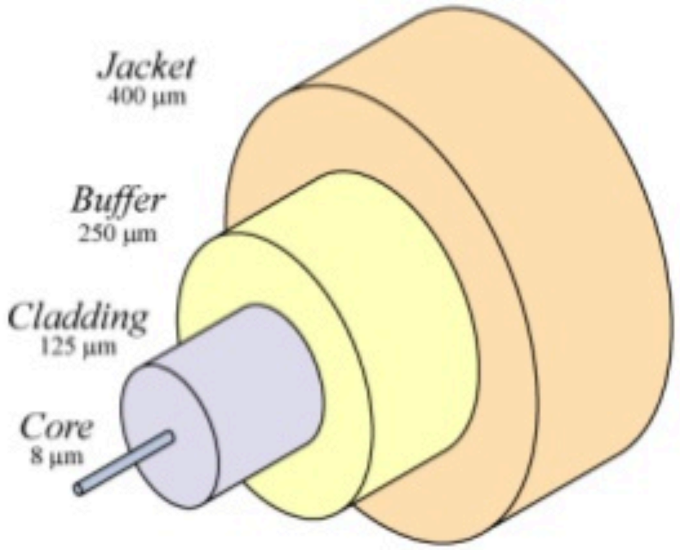
Prize motivation: "for groundbreaking achievements concerning the transmission of light in fibers for optical communication"

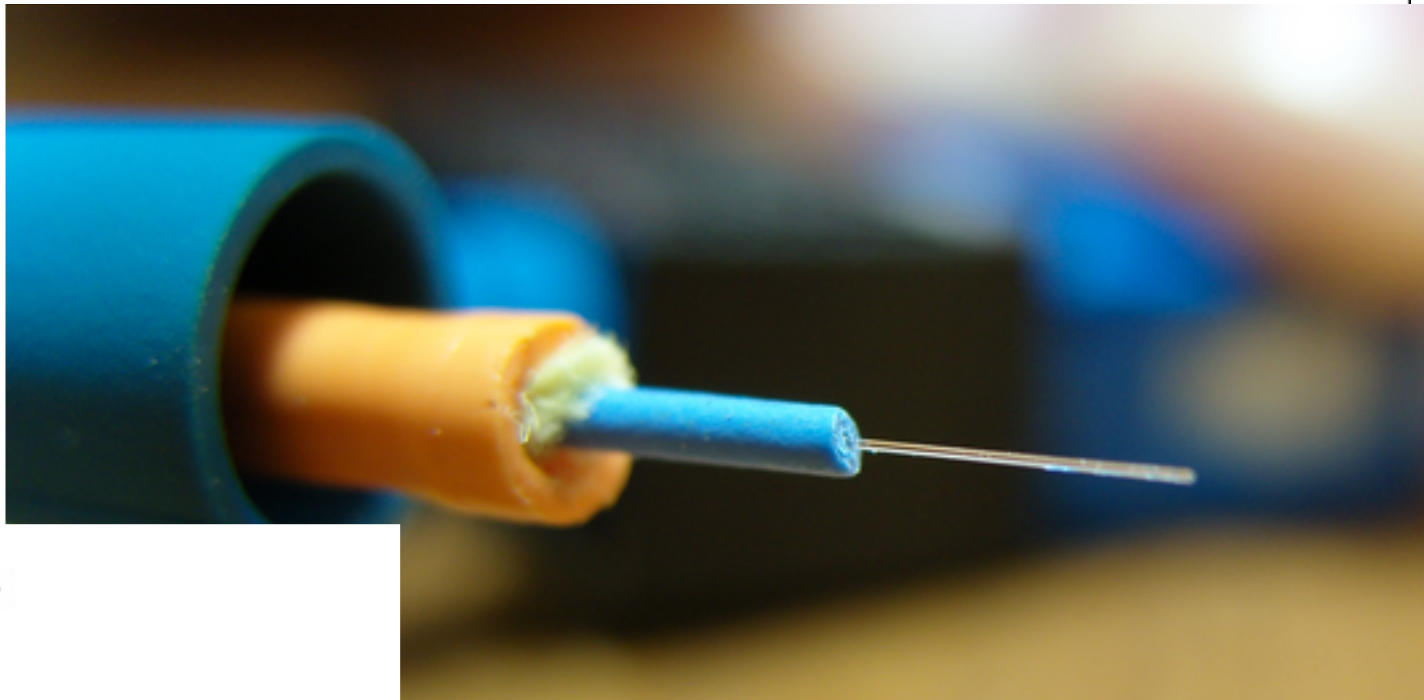
Field: fiber technology, instrumentation

Prize share: 1/2

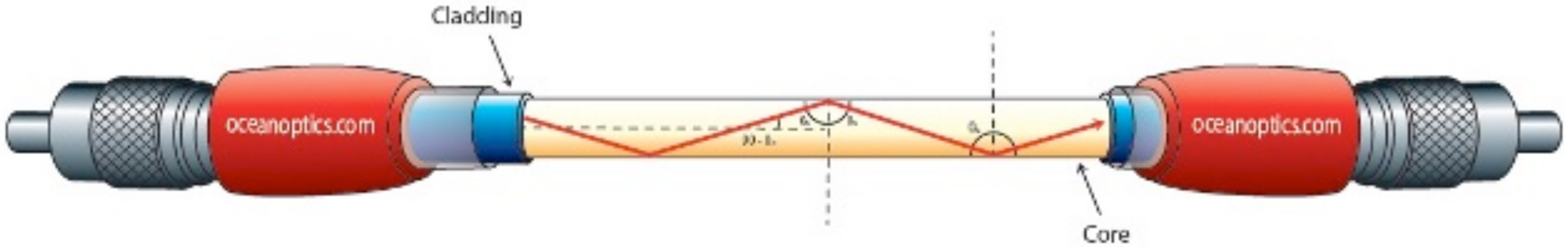
Optical Fiber

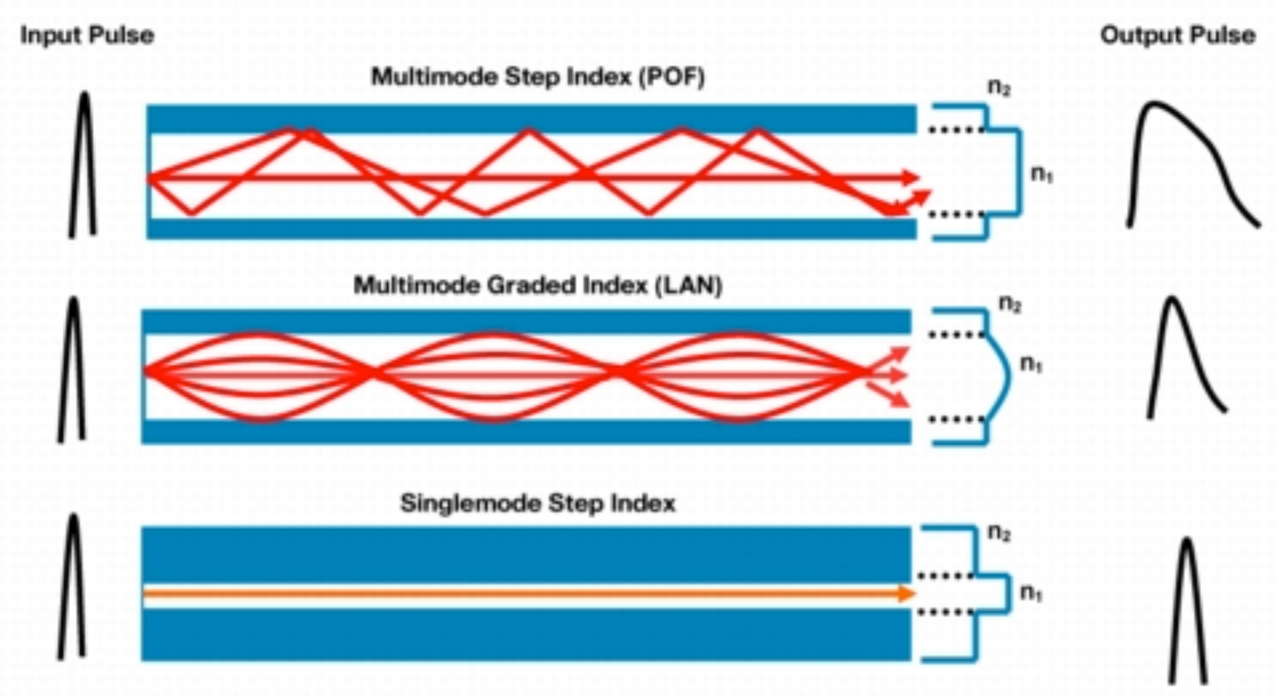
- Core
  - Glass or plastic with a higher index of refraction than the cladding
  - Carries the signal
- Cladding
  - Glass or plastic with a lower index of refraction than the core
- Buffer
  - Protects the fiber from damage and moisture
- Jacket
  - Holds one or more fibers in a cable

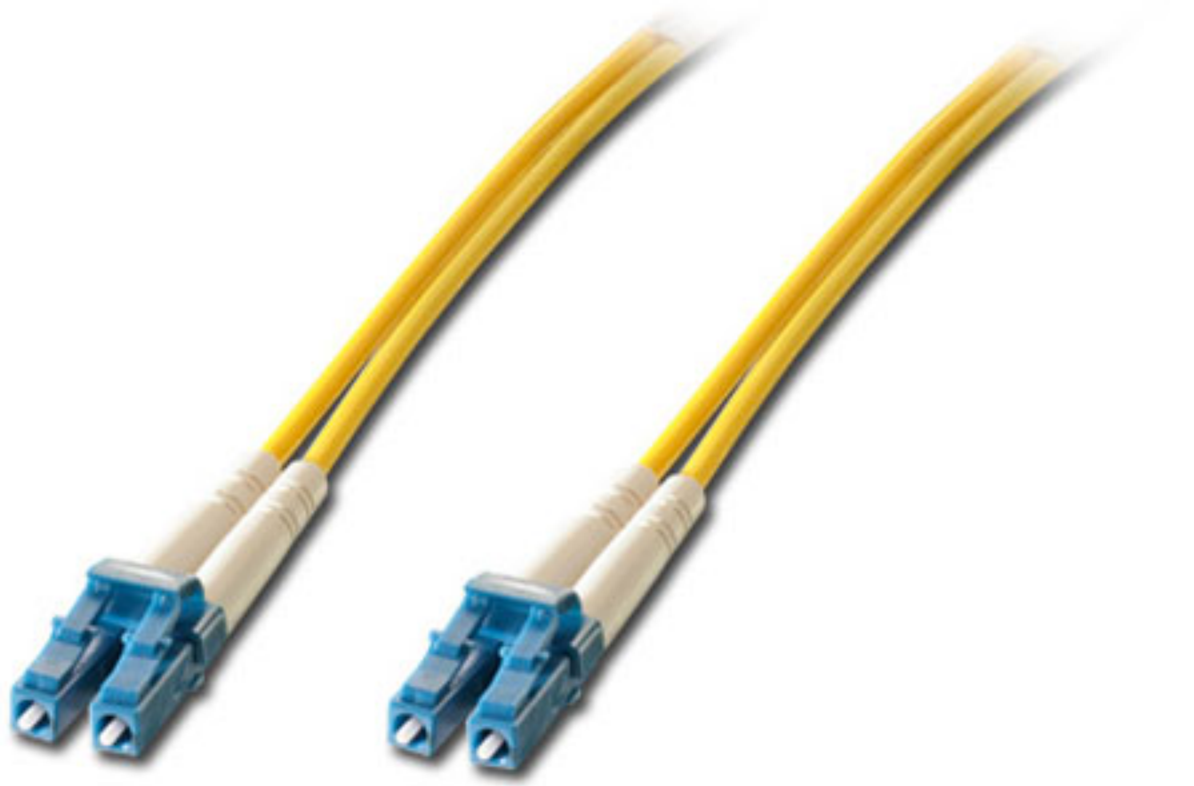




Light Passing Through an Optical Fiber

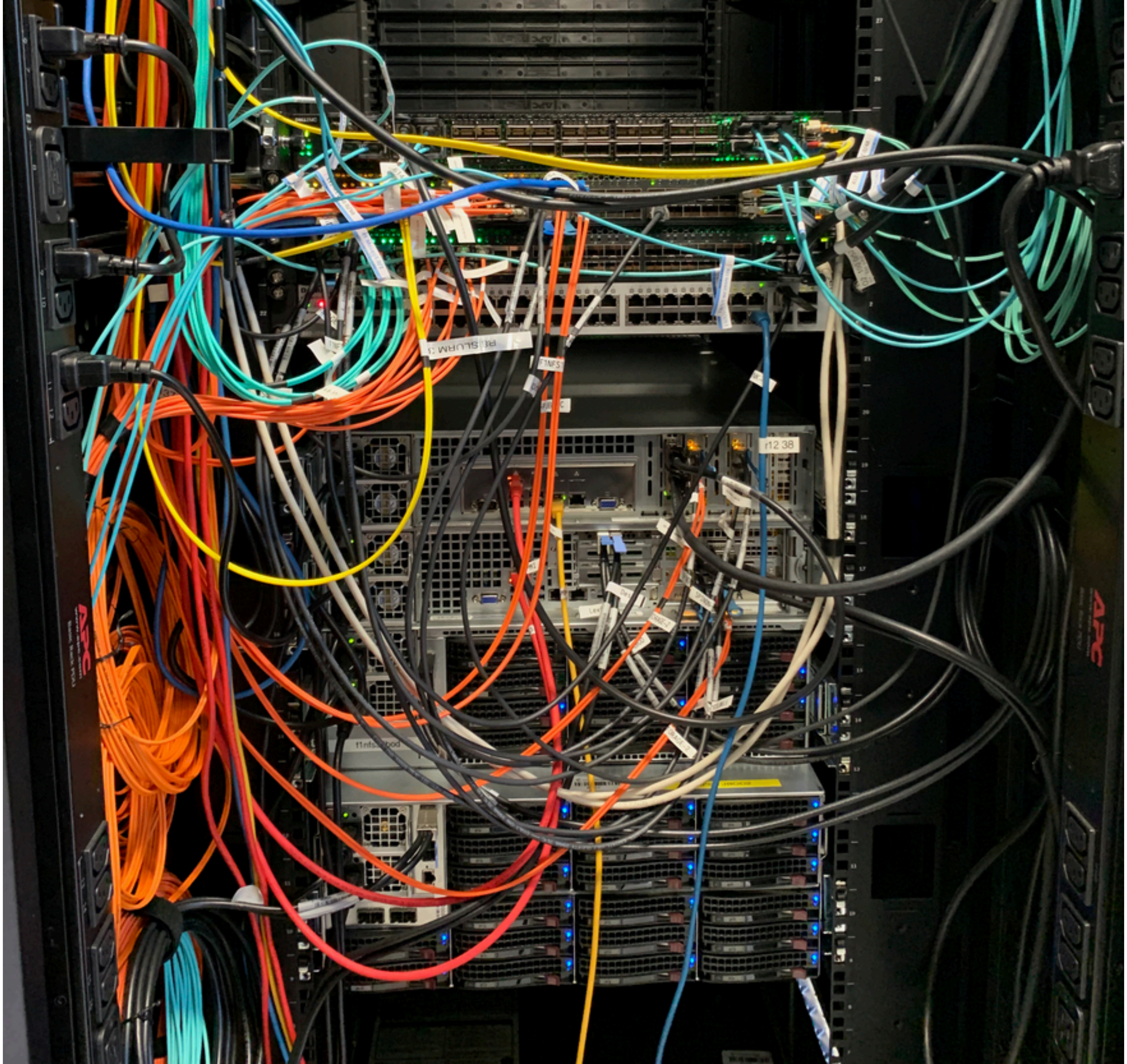




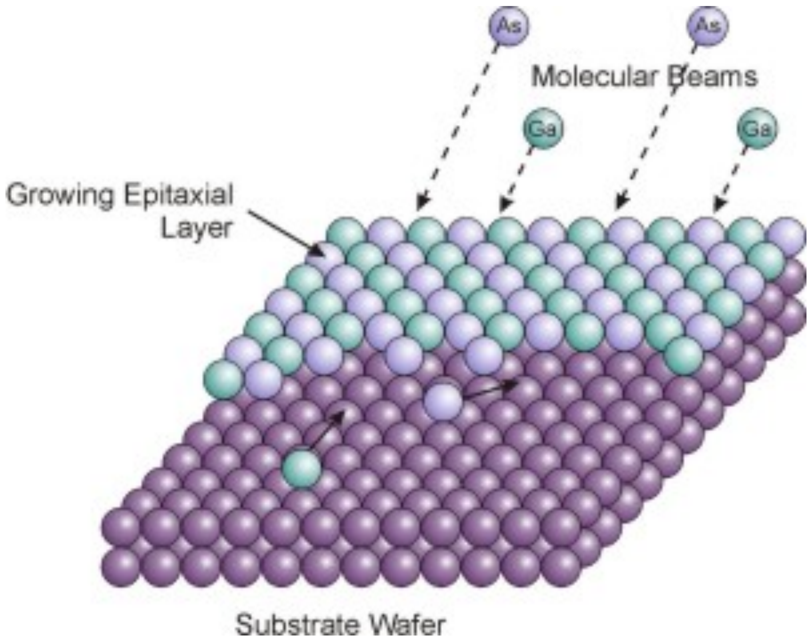


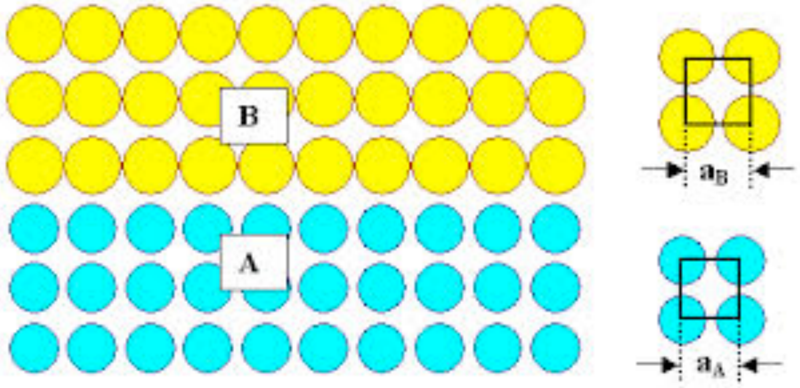
	Mode	Core Diameter	Wavelength	Modal Bandwidth	Cable jacket color
OM1	multi-mode	62.5 µm	850 nm 1300 nm	200 MHz	Orange
OM2	multi-mode	50 µm	850 nm 1300 nm	500 MHz	Orange
OM3	multi-mode	50 µm	850 nm 1300 nm	2000 MHz	Aqua
OM4	multi-mode	50 µm	850 nm 1300 nm	4700 MHz	Aqua
OS1	single-mode	9 µm	1310 nm 1550 nm	—	Yellow

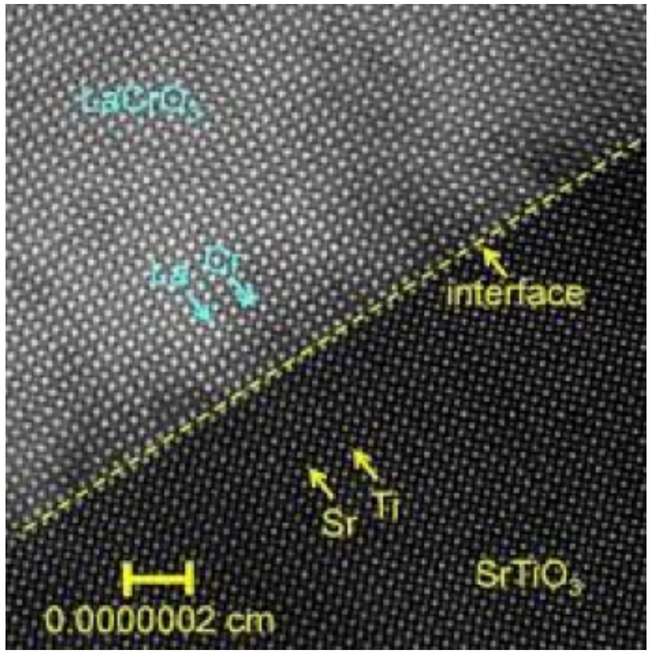

INROW 6
APC

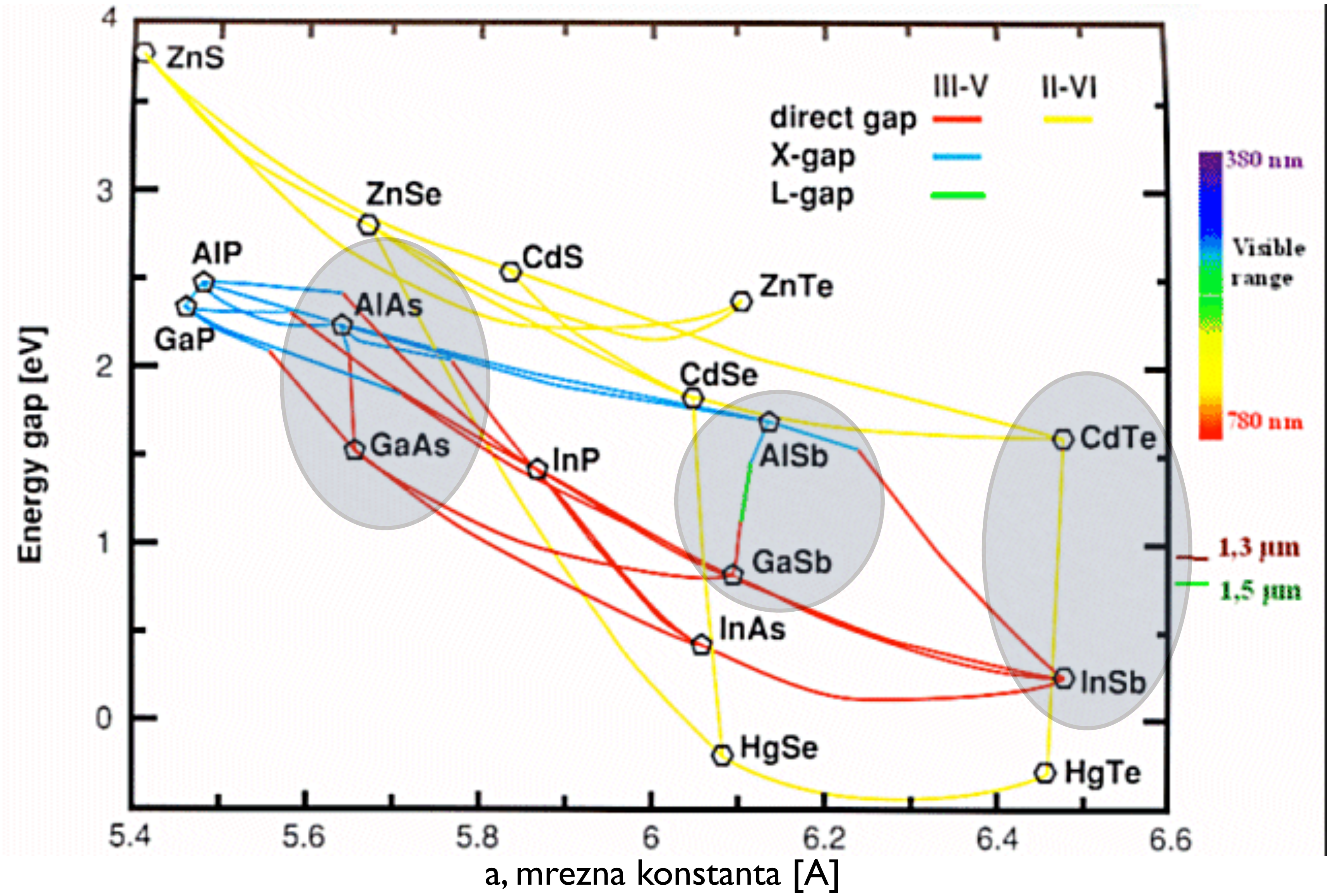

APC
r12 38
APC

HETEROSTRUKTURE


As
As
Molecular Beams
Ga
Ga
Growing Epitaxial Layer
Substrate Wafer


B
A
a_B
a_A


LaCrO$_3$
La
Cr
interface
Sr
Ti
SrTiO$_3$
0.0000002 cm

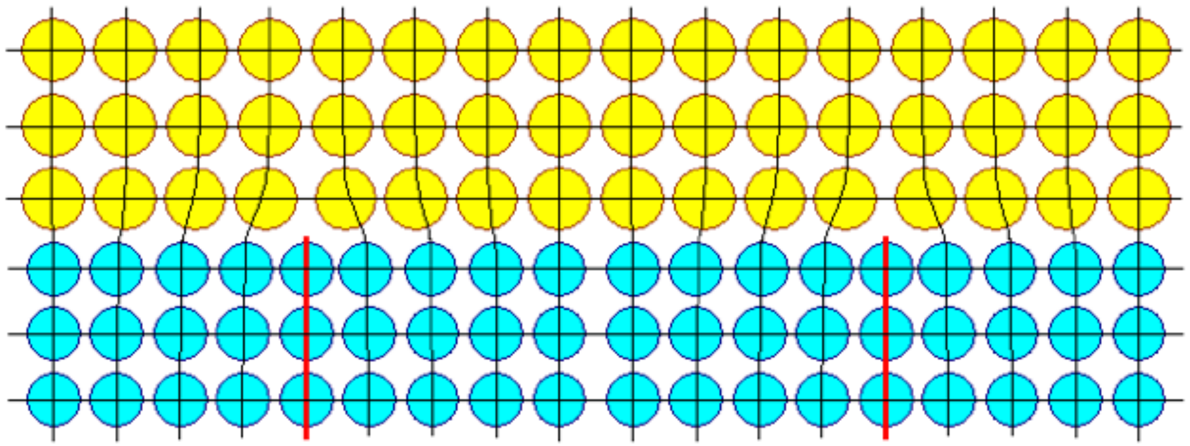


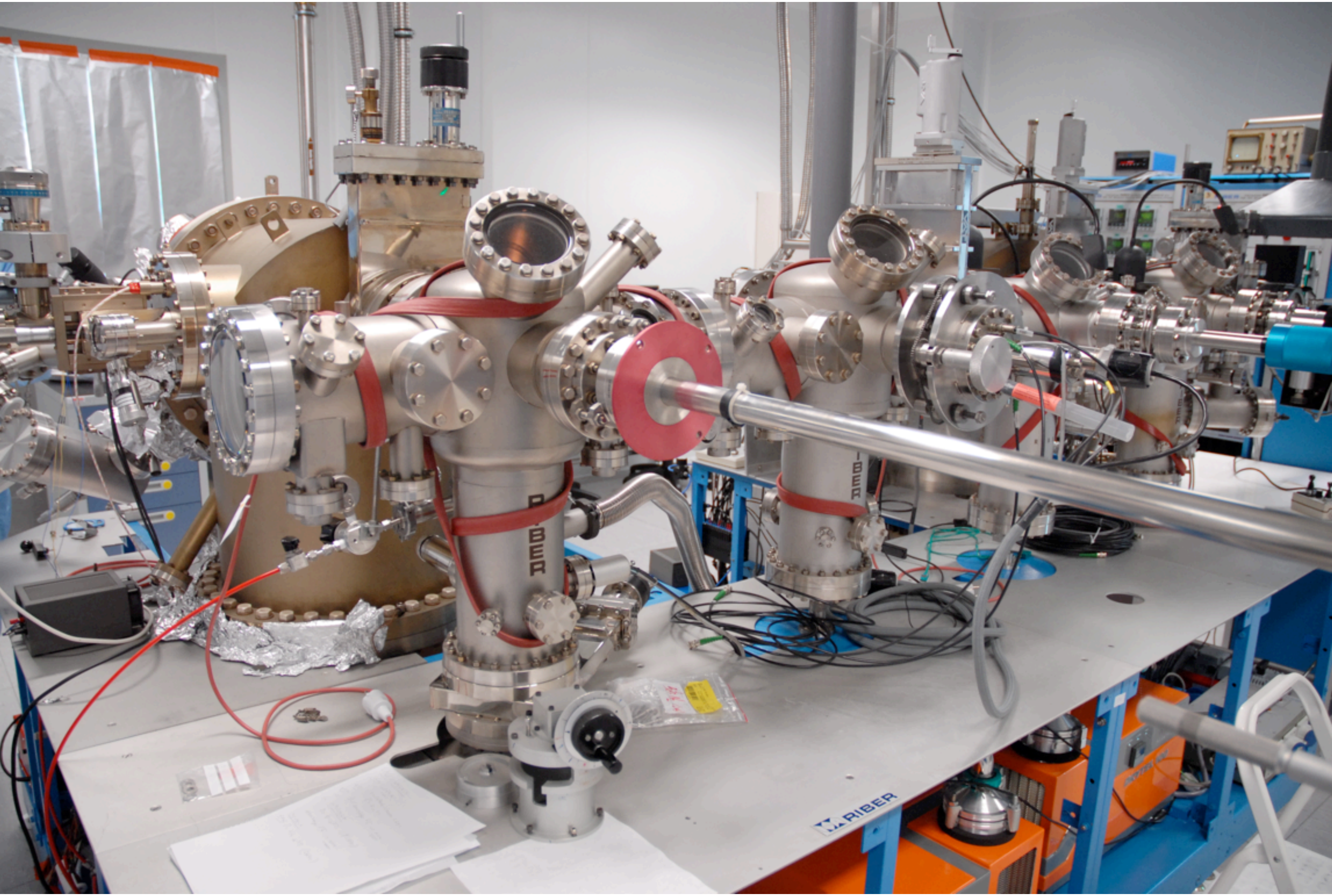
$Al_xGa_{1-x}As$

$x=0 \quad E_g=1.4eV$

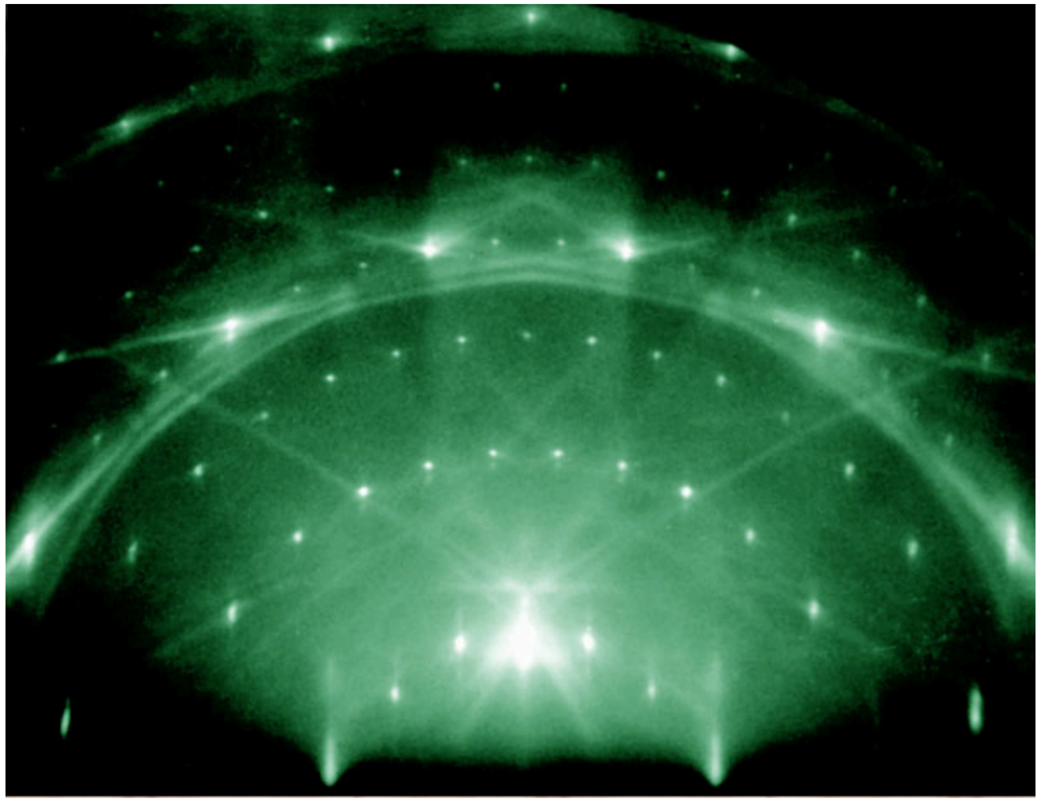
$x=1 \quad E_g=2.2eV$

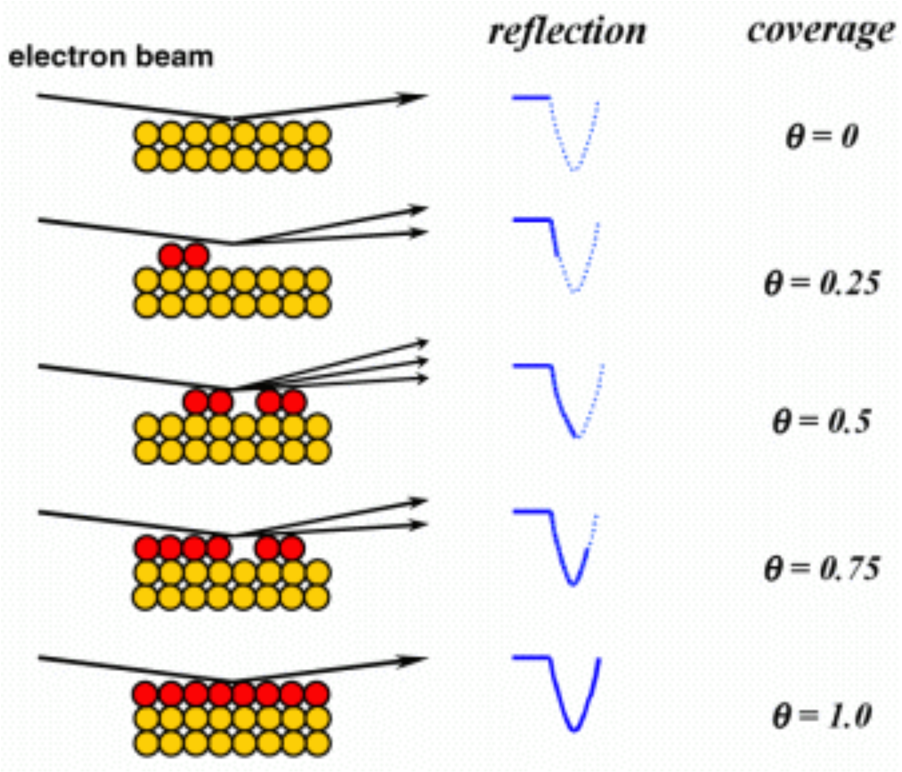
$Ga_xIn_{1-x}As_yP_{1-y}$

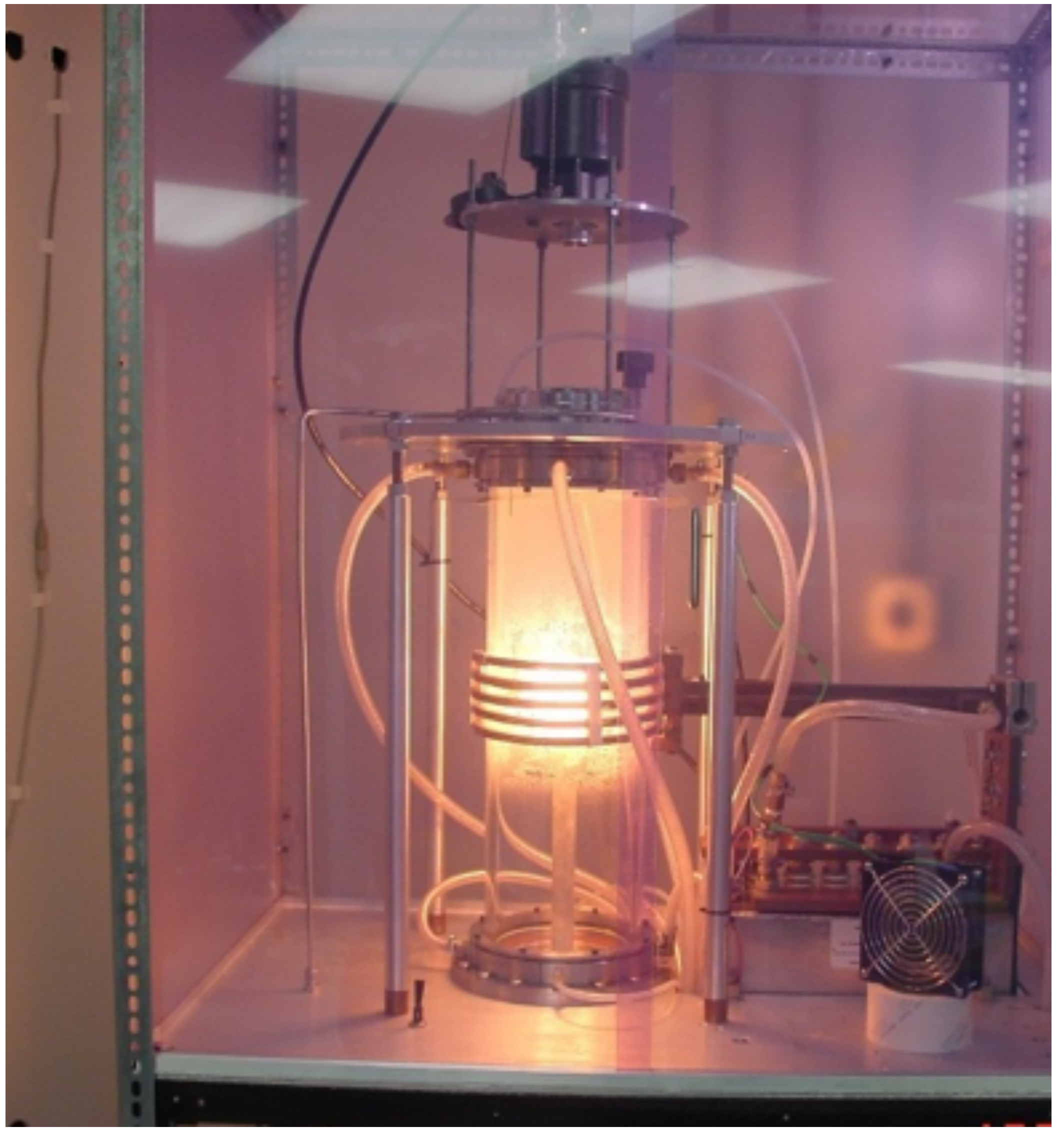


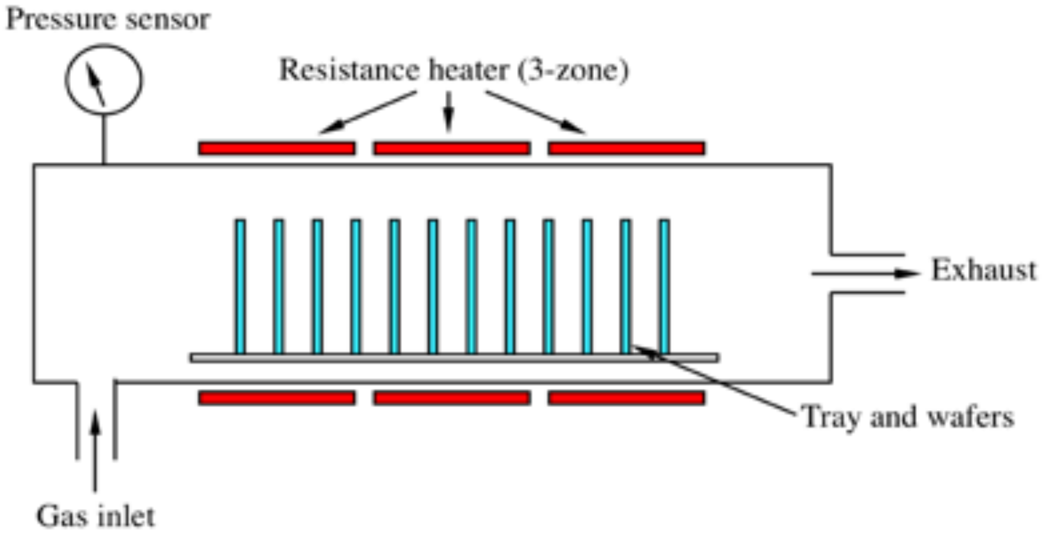

RIBER
RIBER
RIBER

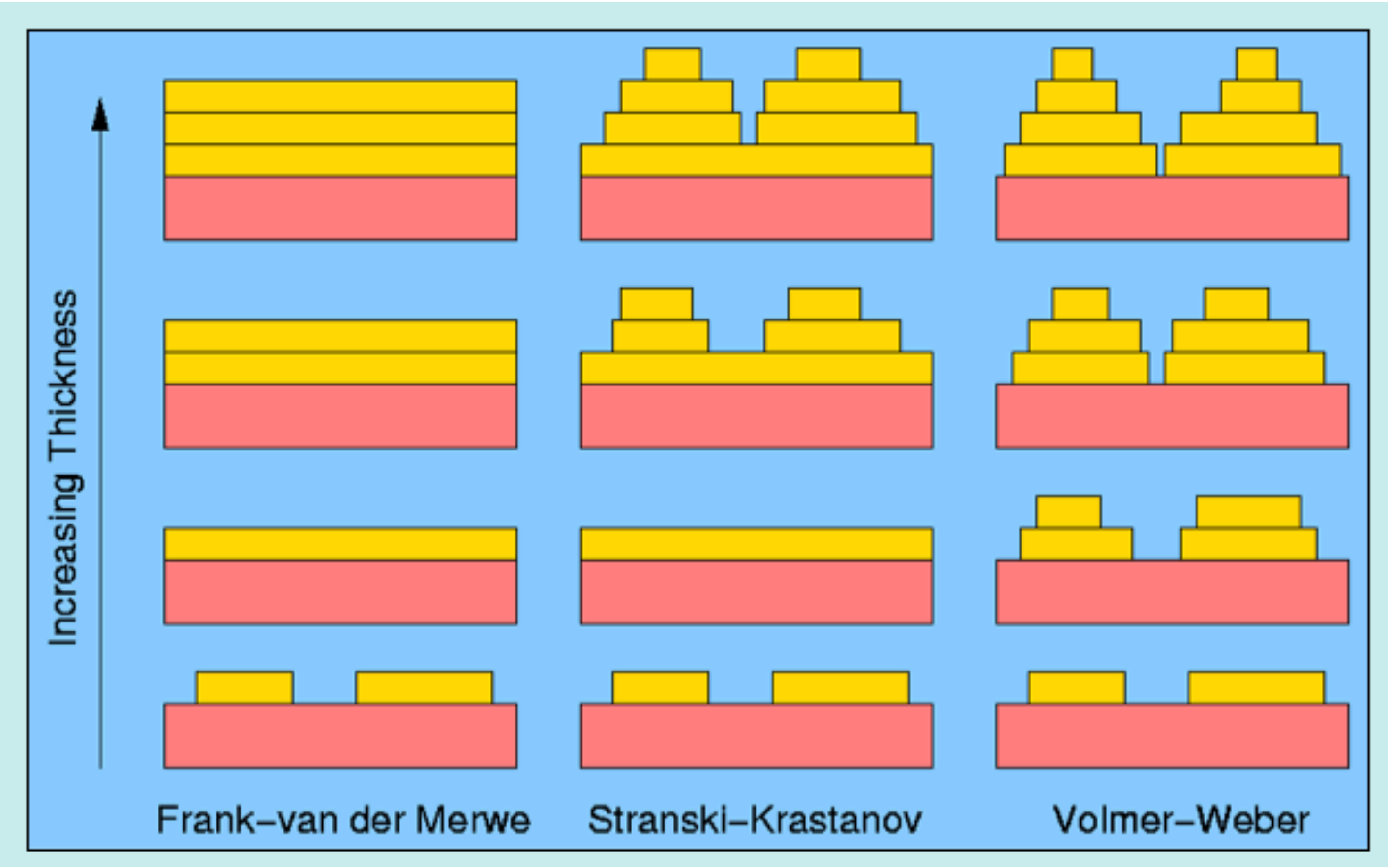
RHEED

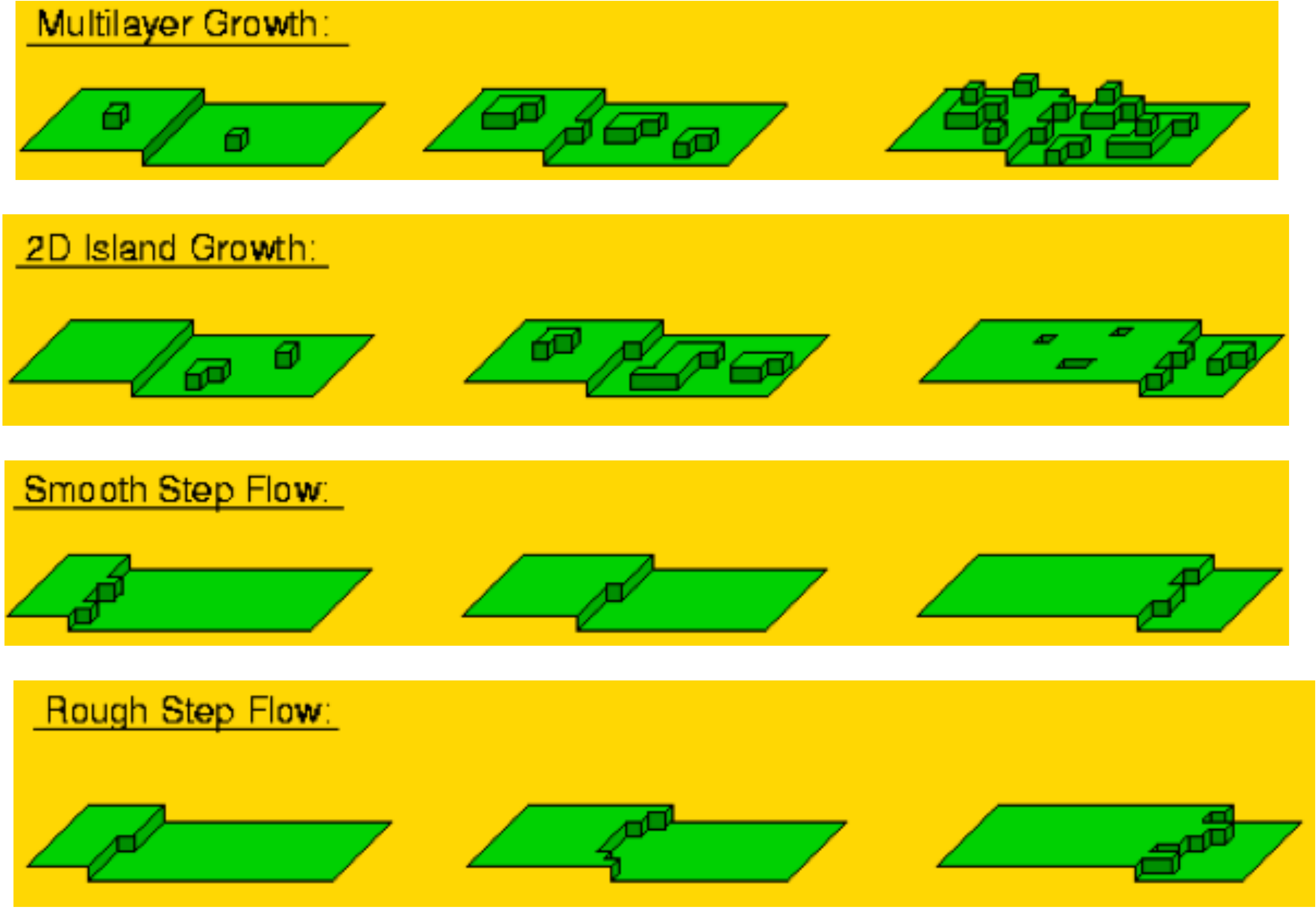


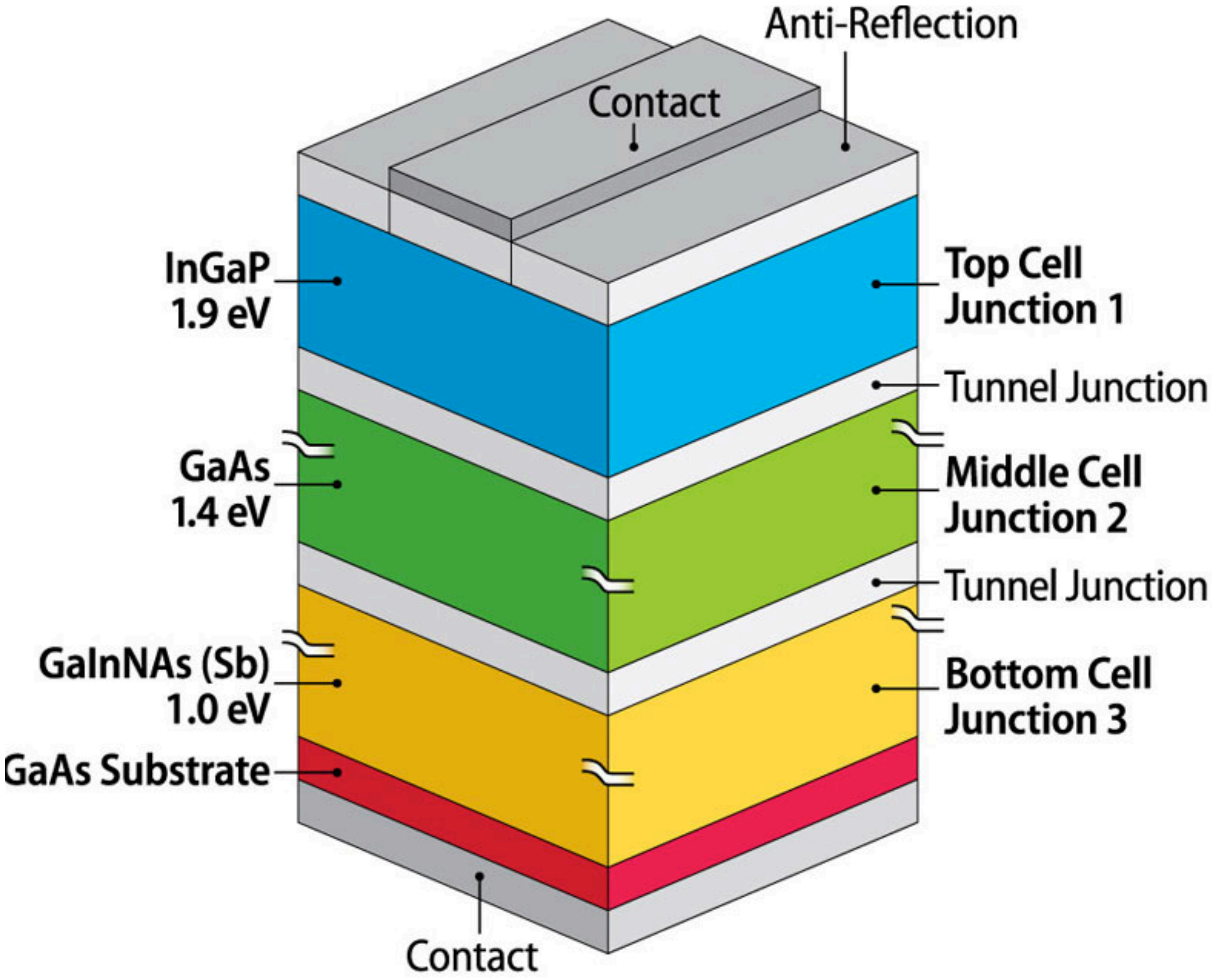


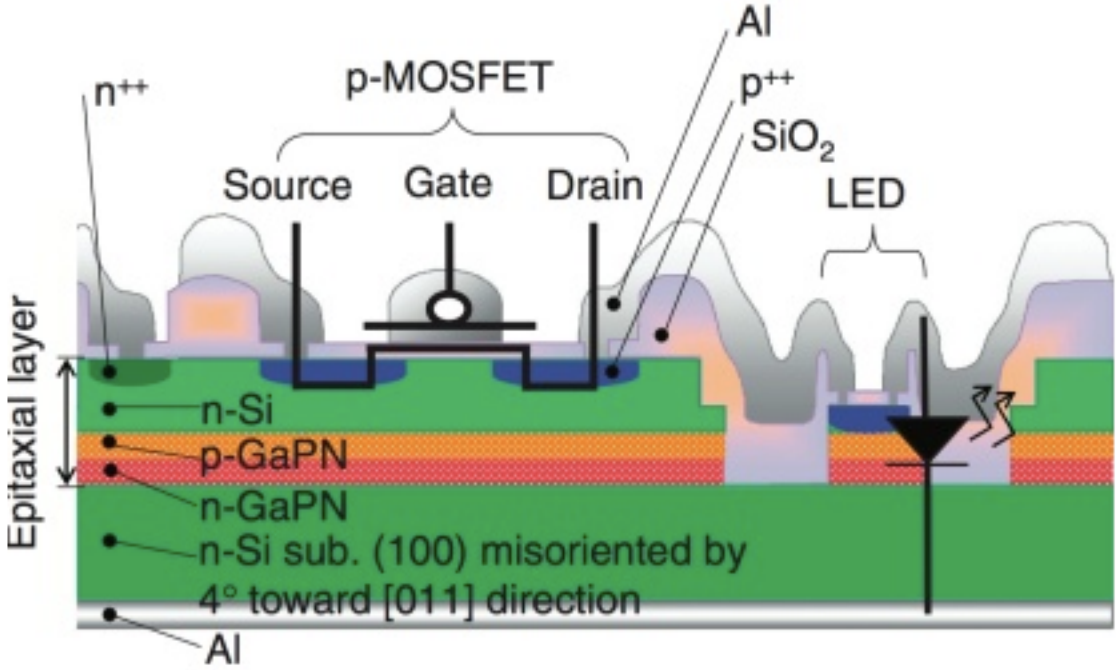



Pressure sensor
Resistance heater (3-zone)
Exhaust
Tray and wafers
Gas inlet


Increasing Thickness
Frank–van der Merwe
Stranski–Krastanov
Volmer–Weber


Multilayer Growth:
2D Island Growth:
Smooth Step Flow:
Rough Step Flow:





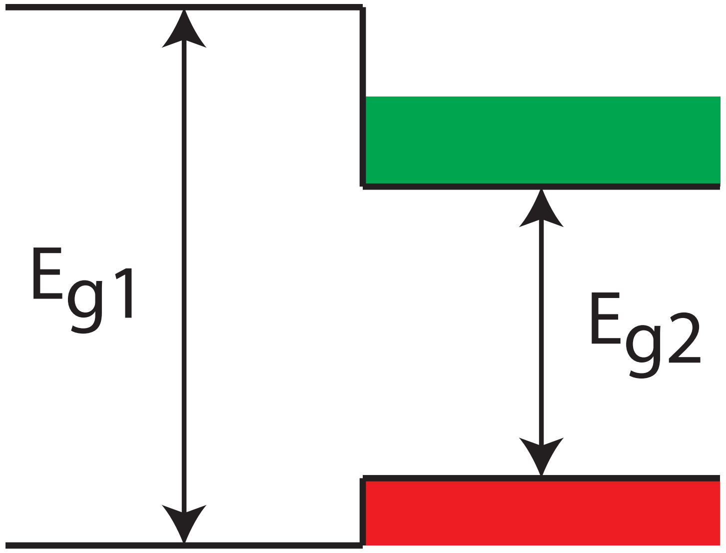
sončna celica

integracija GaAs s Si

Zhores Ivanovich Alferov (Russian: Жорéс Ивáнович Алфёров, [ʐɐˈrʲɛs ɪˈvanəvʲɪtɕ ɐlʲˈfʲorəf]; Belarusian: Жарэс Iвáнавіч Алфёраў; born March 15, 1930) is a Belarusian, Soviet and Russian physicist and academic who contributed significantly to the creation of modern heterostructure physics and electronics. He is the inventor of the heterotransistor and the winner of 2000 Nobel Prize in Physics. He is also a Russian politician and has been a member of the Russian State Parliament, the Duma, since 1995. Lately, he has become one of the most influential members of the Communist Party of the Russian Federation.

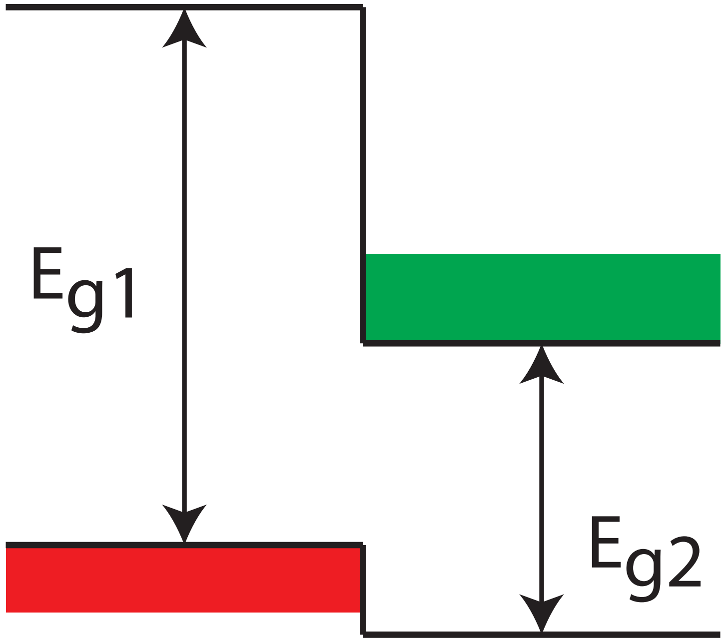
Born	Zhores Ivanovich Alferov 15 March 1930[1] Vitebsk, Byelorussian SSR, Soviet Union[1]
Died	1 March 2019 (aged 88)[1] St Petersburg, Russia[1]
Nationality	Soviet (until 1991) / Russian (since 1991)
Alma mater	Saint Petersburg State Electrotechnical University "LETI" (old name V. I. Ulyanov Electrotechnical Institute "LETI")
Known for	Heterotransistors
Awards	Global Energy Prize (2005) Kyoto Prize in Advanced Technology (2001) Nobel Prize in Physics (2000) Demidov Prize (1999) Ioffe Prize (Russian Academy of Sciences, 1996) USSR State Prize (1984) Lenin Prize (1972) Stuart Ballantine Medal (1971) Order of Lenin (1986)
Scientific career	
Fields	Applied physics
Institutions	Ioffe Physico-Technical Institute
Thesis	*Heterojunctions in semiconductors* (1970)

HETEROSPOJ



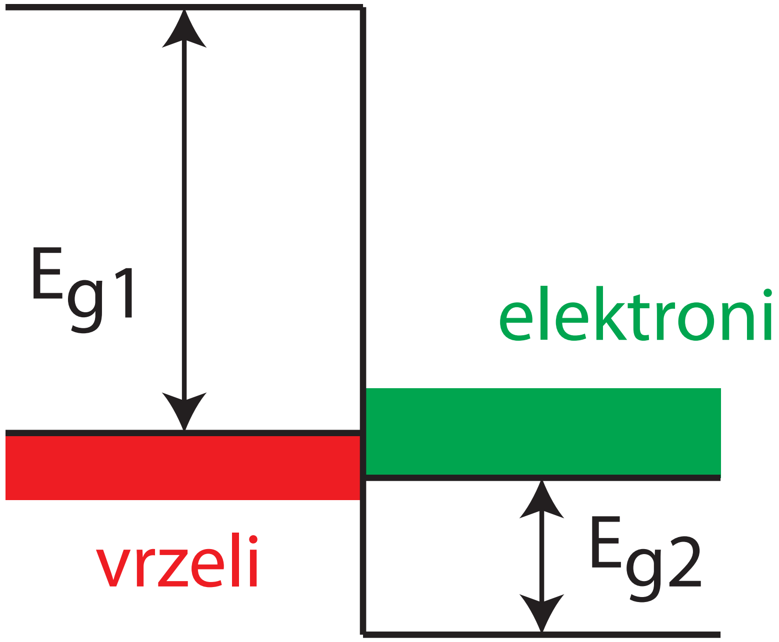
I: povezan tip

GaAlAs/GaAs



II: zamaknjen tip

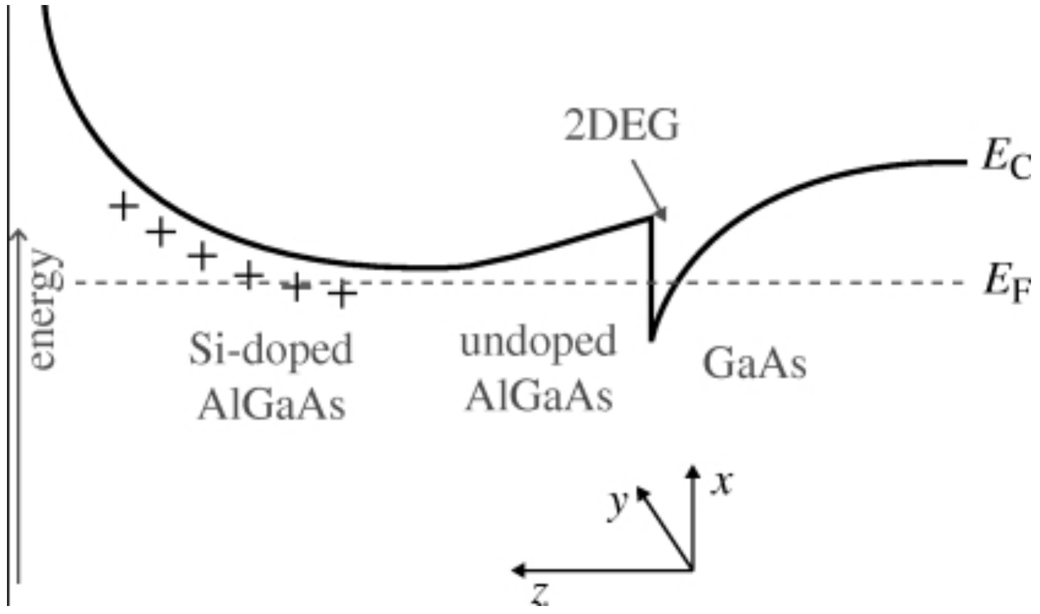
InAs/Al$_{0.4}$Ga$_{0.6}$Sb



III: prekinjen tip

InAs/GaSb

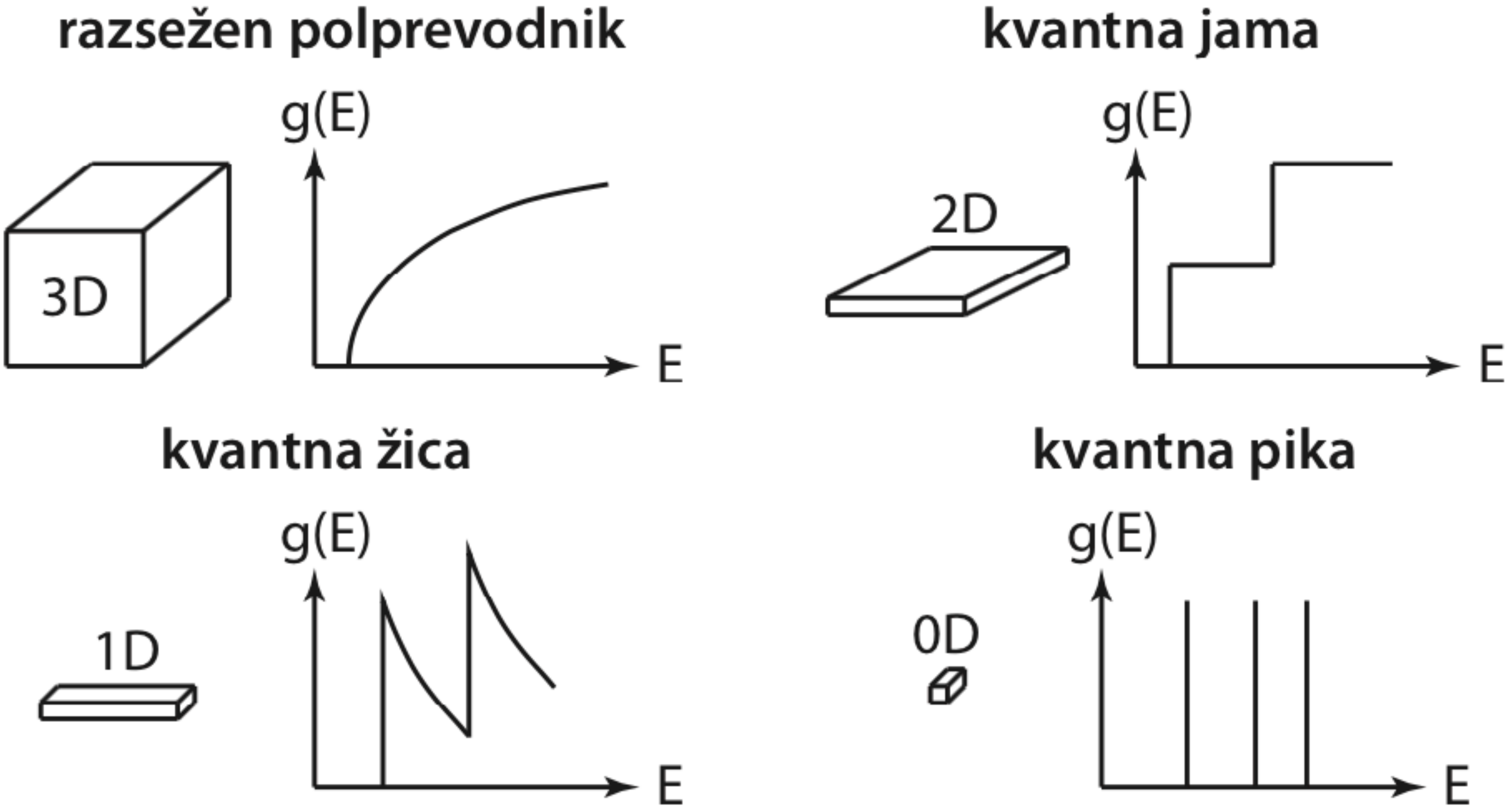
DVODIMENZIONALNI ELEKTRONSKI PLIN



debelina: 10 nm

gostota elektronov: $10^{11}/cm^2$

GOSTOTA STANJ V 3D, 2D, 1D, 0D SISTEMIH



razsežen polprevodnik

kvantna jama

kvantna žica

kvantna pika

3D

$$\frac{4\pi}{3}k_F^3 = \frac{N}{2}\frac{(2\pi)^3}{V}$$

$$E_F = \frac{\hbar^2}{2m_e}k_F^2 = \frac{\hbar^2}{2m_e}\left(3\pi^2 n\right)^{2/3}$$

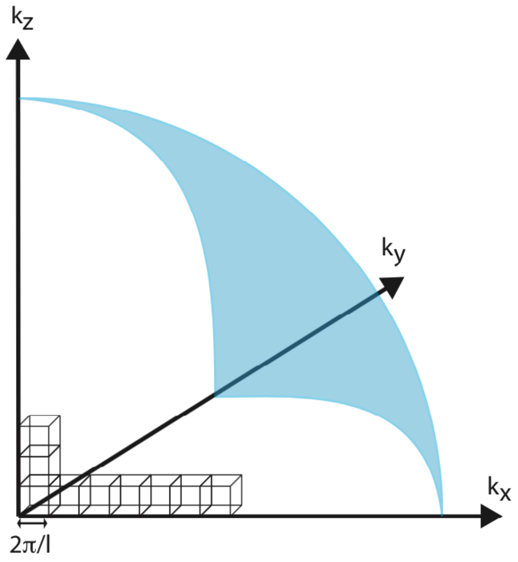
$$g(E) = \frac{\mathrm{d}N(E)}{\mathrm{d}E} \propto E^{1/2}$$

2D

$$\frac{N}{2}\frac{(2\pi)^2}{S} = \pi k_F^2$$

$$E_F = \frac{\hbar^2}{2m_e}2\pi n$$

$$g(E) = \frac{\mathrm{d}N(E)}{\mathrm{d}E} = \frac{m_e}{\pi\hbar^2}S = \mathrm{konst}$$



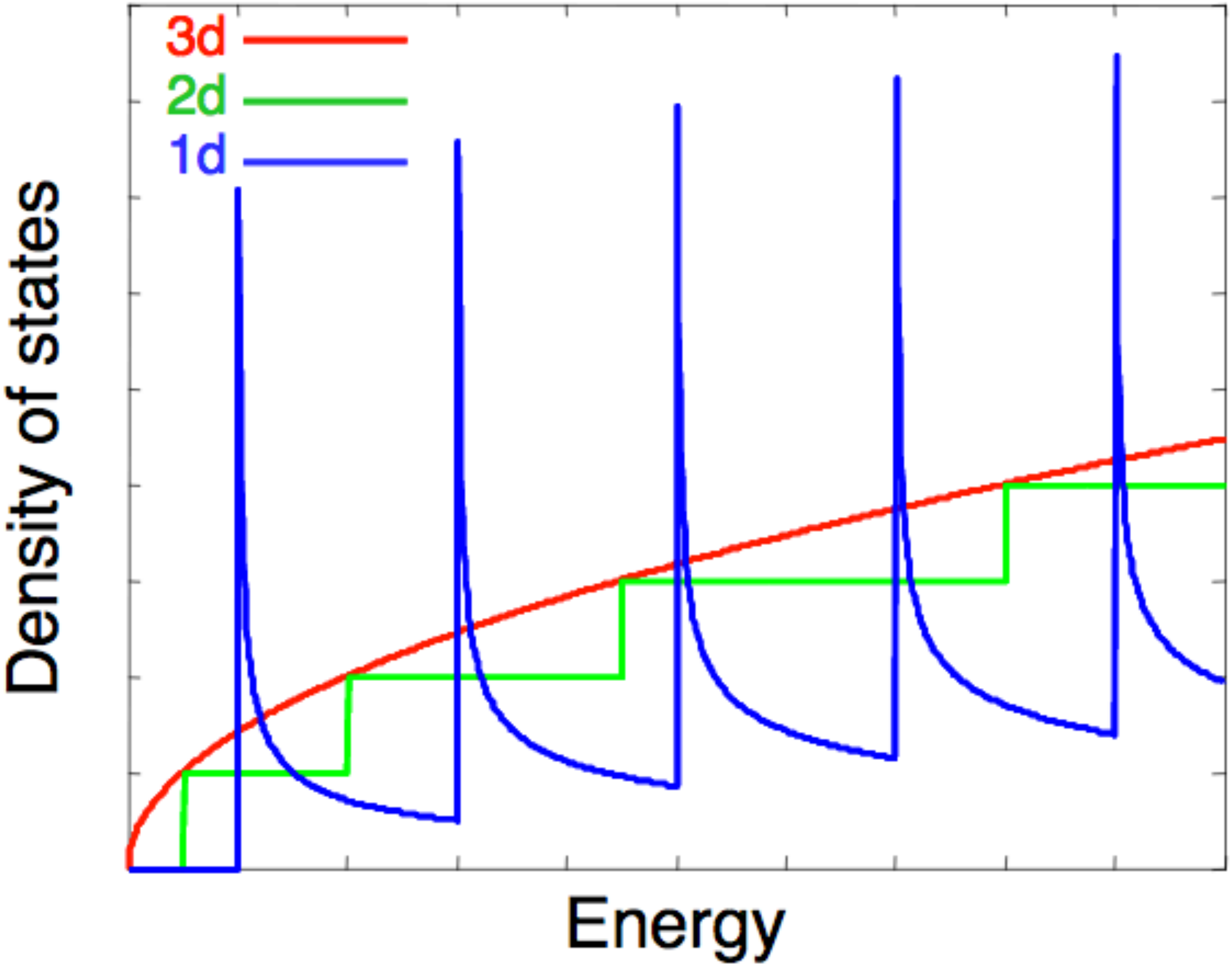
1D

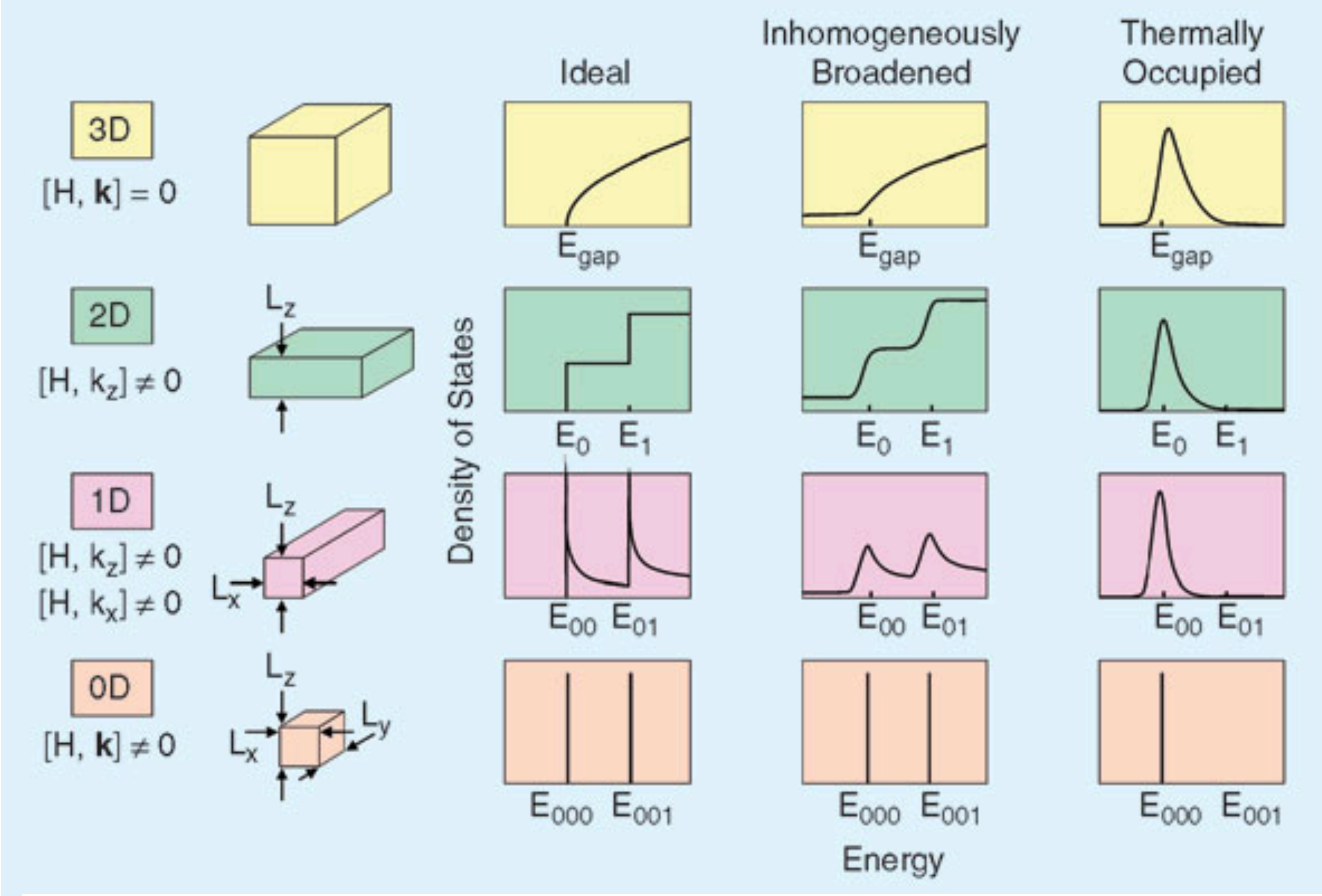
$$\frac{N}{2}\frac{2\pi}{l} = 2k_F$$

$$E_F = \frac{\hbar^2}{2m_e}(\pi n/2)^2$$

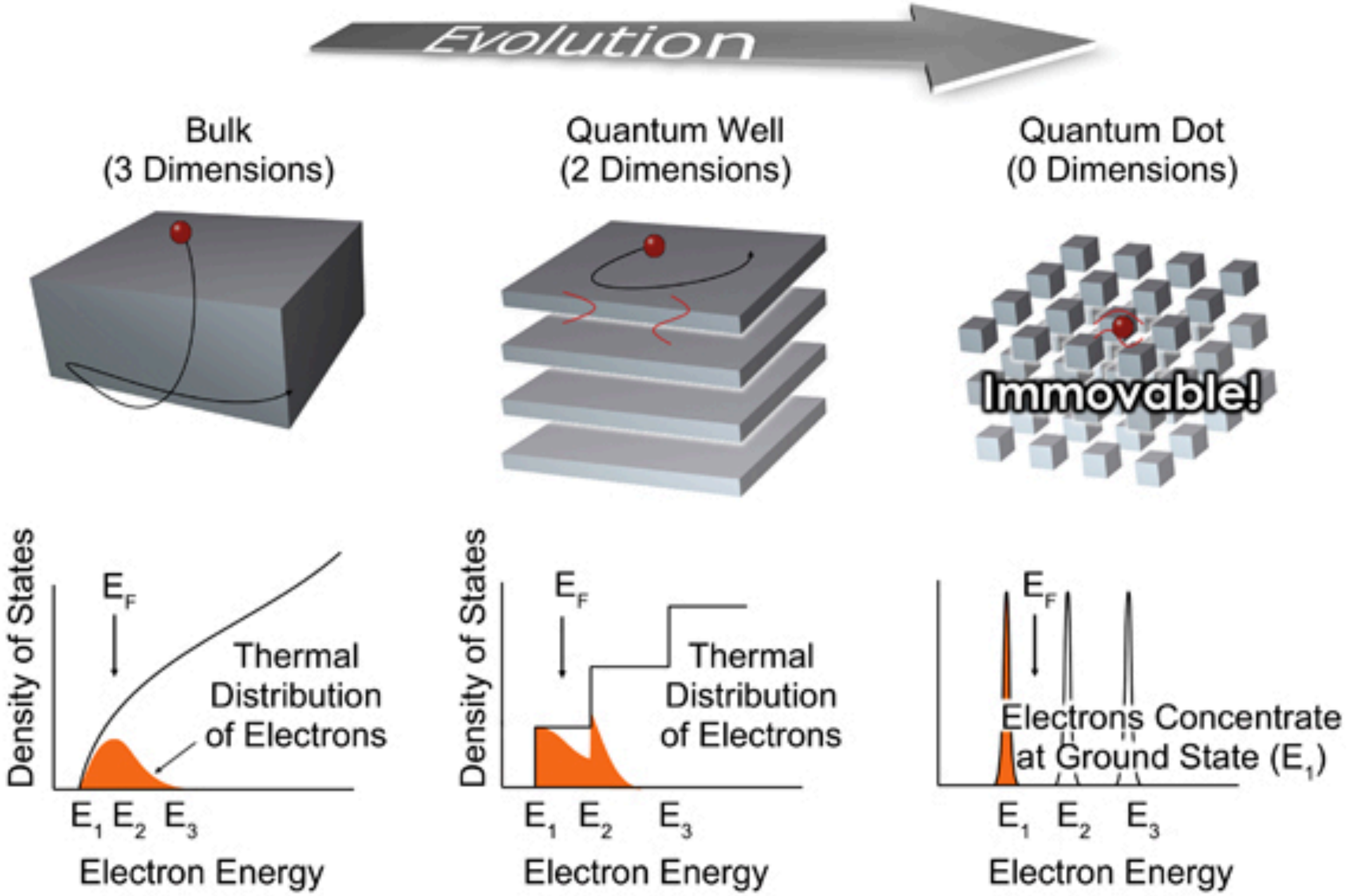
$$g(E) = \frac{\mathrm{d}N(E)}{\mathrm{d}E} = l\frac{\sqrt{2m_e}}{\hbar}\frac{1}{\pi}\frac{1}{\sqrt{E}}$$

$$g(E) = \frac{4l}{hv}$$

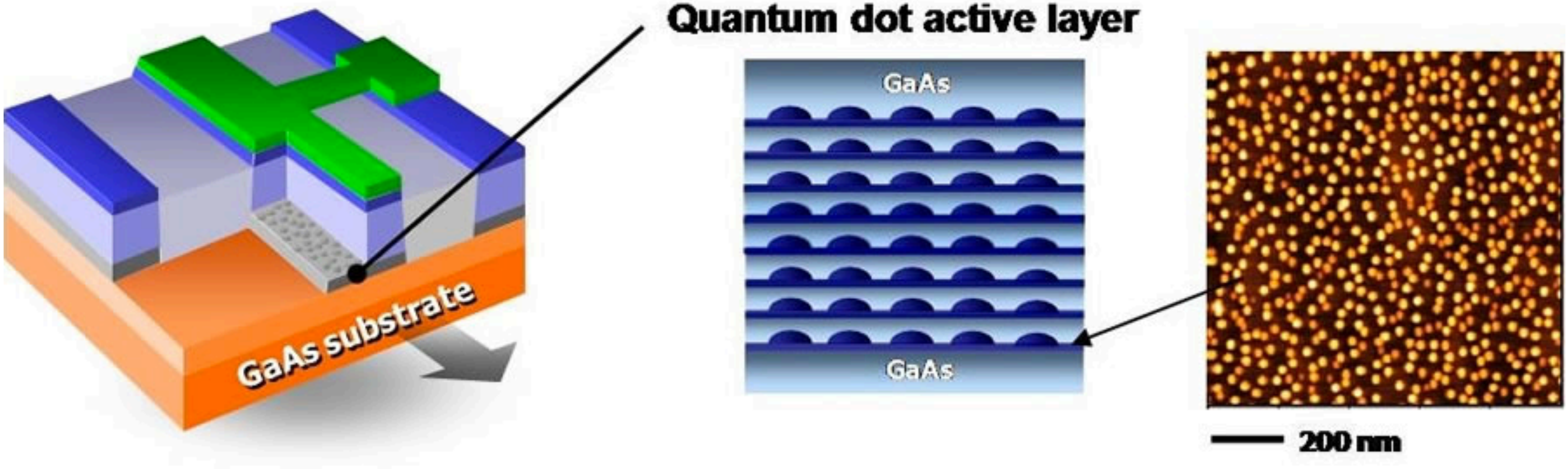

3d
2d
1d
Density of states
Energy



Ideal
Inhomogeneously Broadened
Thermally Occupied
3D
$[H, \mathbf{k}] = 0$
2D
$[H, k_z] \neq 0$
1D
$[H, k_z] \neq 0$
$[H, k_x] \neq 0$
0D
$[H, \mathbf{k}] \neq 0$
L_z
L_x
L_y
Density of States
E_{gap}
E_0 E_1
E_{00} E_{01}
E_{000} E_{001}
Energy



Evolution
Bulk (3 Dimensions)
Quantum Well (2 Dimensions)
Quantum Dot (0 Dimensions)
Immovable!
Density of States
E_F
Thermal Distribution of Electrons
Electrons Concentrate at Ground State (E_1)
E_1 E_2 E_3
Electron Energy


Quantum dot active layer
GaAs
GaAs
GaAs substrate
200 nm