

POVZETNA IDEJA

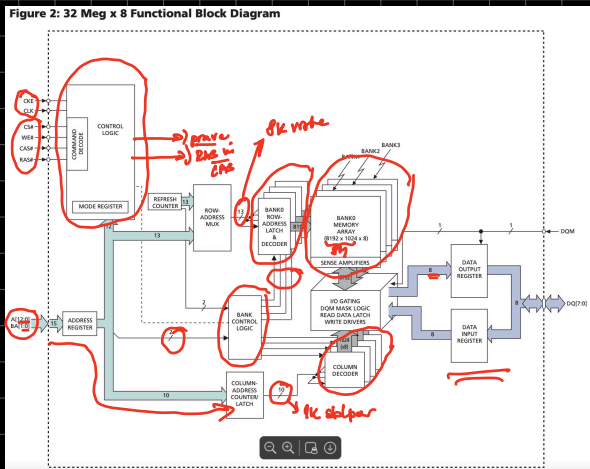
→ NE ZAPIRAM Vrstice! (vber: A iste vrste
 ↓
 potratni prostorilo
 tu osnovno (obalovst)

→ skušamo stolpce pobirati tako, da
 prepletamo naslavljanje stolpca in
 branje A stolpca

↳ "Natančno upravljanje s časom"
 → v DRAM uprednostimo logiko, ki bo prepletala
 te dve

→ POTROŠNOSTIHO VIRSNIK :
 tisti ki naslavlja RAM, le temu parcu "UKAZ"

⇓
USETO : SDRAM



x8	x16	x16	x8		
-	VDD	1	54	VSS	-
DQ0	DQ0	2	53	DQ15	DQ7
-	VDDQ	3	52	VSSQ	-
NC	DQ1	4	51	DQ14	NC
DQ1	DQ2	5	50	DQ13	DQ6
-	VSSQ	6	49	VDDQ	-
NC	DQ3	7	48	DQ12	NC
DQ2	DQ4	8	47	DQ11	DQ5
-	VDDQ	9	46	VSSQ	-
NC	DQ5	10	45	DQ10	NC
DQ3	DQ6	11	44	DQ9	DQ4
-	VSSQ	12	43	VDDQ	-
NC	DQ7	13	42	DQ8	NC
-	VDD	14	41	VSS	-
NC	DQM1	15	40	NC	-
-	WE#	16	39	DQM#	DQM
-	CAS#	17	38	CLK	-
-	RAS#	18	37	CKE	-
-	CS#	19	36	A12	-
-	BA0	20	35	A11	-
-	BA1	21	34	A9	-
-	A10	22	33	A8	-
-	A0	23	32	A7	-
-	A1	24	31	A6	-
-	A2	25	30	A5	-
-	A3	26	29	A4	-
-	VDD	27	28	VSS	-

Table 14: Truth Table - Commands and DQM Operation

Note 1 applies to all parameters and conditions

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	H	H	L	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	8
Write enable/output enable	X	X	X	X	L	X	Active	9
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	9

Eksploriraj: prenos (BURST)

↳ ko želimo brzoje iz eneje sklopke iz odpote vrstice, mi RAM tako vrne namizt 1 besede 1, 2, 3, 4, 5, ... "sosednjih besed"

↓
dolžina eksplozijskega prenosu (BL)

↳ se jo da nastaviti

↳ t_{CL} jedaj merimo v skleni vrhni period

NASTAJA SE V

MODE register

↳ to nastavi t_{CL}; ko RAM nastane, sledi na sugovno

Figure 19: Mode Register Definition

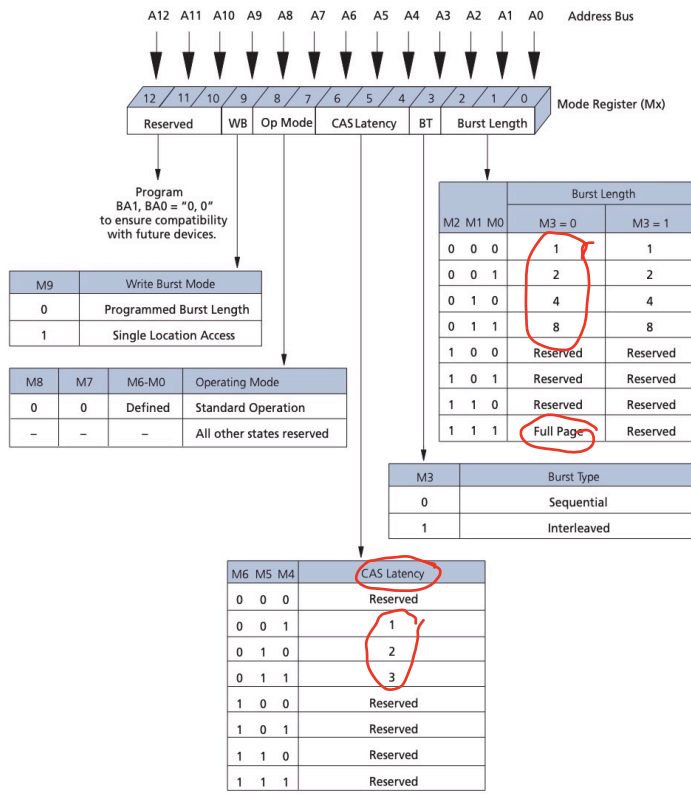


Table 1: Key Timing Parameters

CL = CAS (READ) latency

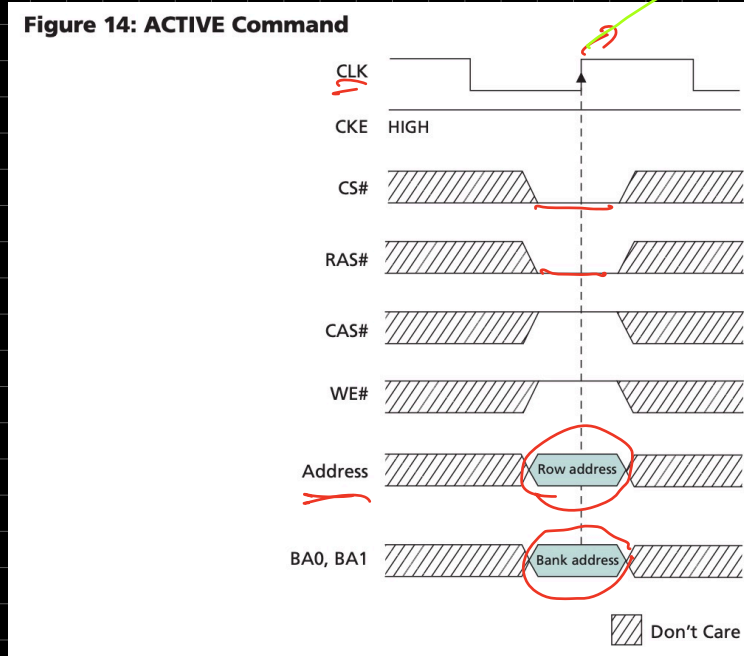
Speed Grade	Clock Frequency (MHz)	Target ^t RCD- ^t RP-CL	^t RCD (ns)	^t RP (ns)	CL (ns)
-6A	167	3-3-3	18	18	18
-75	133	3-3-3	20	20	20
-7E	133	2-2-2	15	15	15

$T_{CLK} = 7.5 ns$

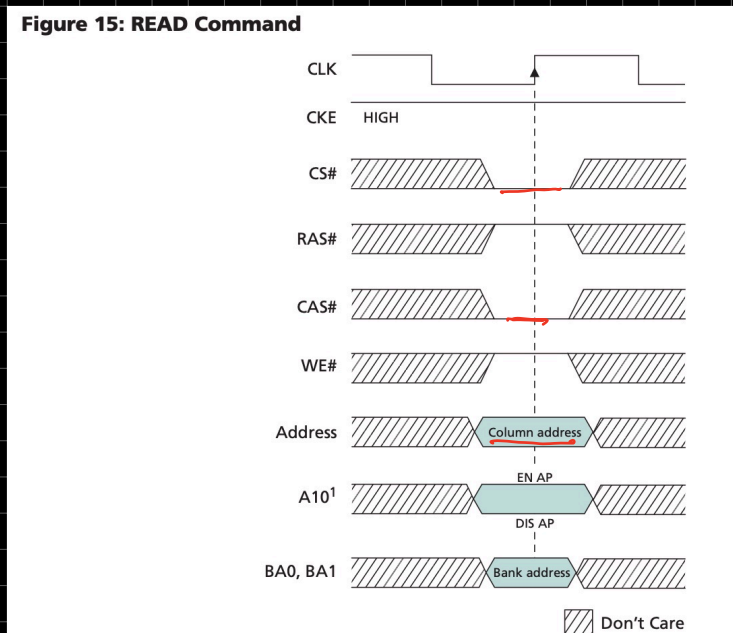
UPORABA

1. ODPIRANJE VRSTICE

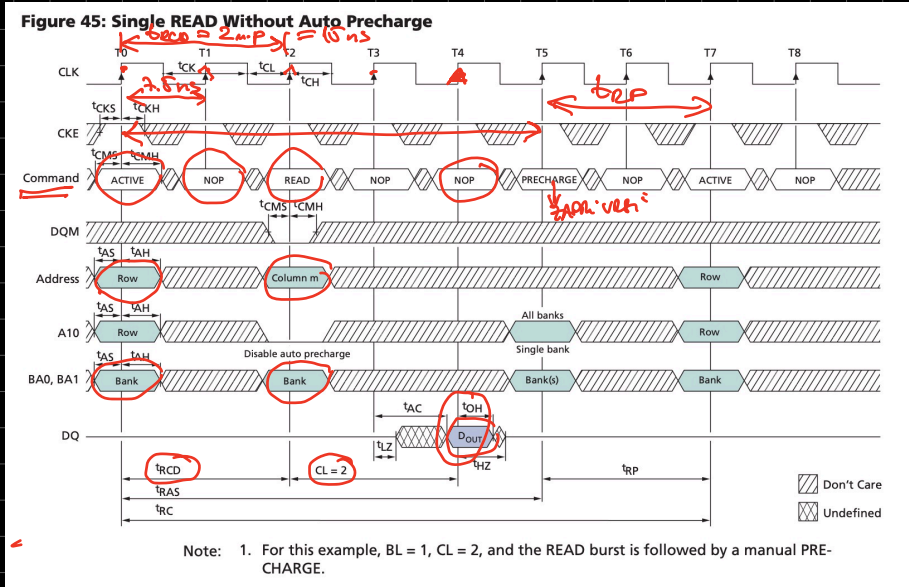
SRAM REGISTRIRA UKAZ



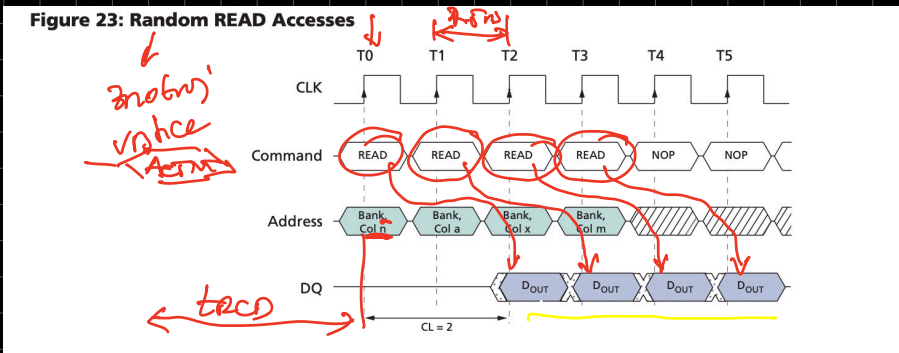
2) PIRANJE STOLPCE (BRANJE)



3) Naključno branje ene besede



$t_{acc} =$
 $t_{RCD} + t_{CL}$
 $+ 1 + t_{RP} =$
 $2 + 2 + 1 + 2 = 7$
 $7 \text{ up} / \text{besede}$
 $105 \text{ ns} / \text{besede}$



$$\begin{aligned}
 t_{access} &= t_{RCD} + CL + 4 + t_{RP} \\
 &= \underset{2}{10} \text{ up} / \underset{2}{4} \text{ besede} \\
 &= 70 \text{ ns} \\
 &\approx 18 \text{ ns} / \text{besede}
 \end{aligned}$$