

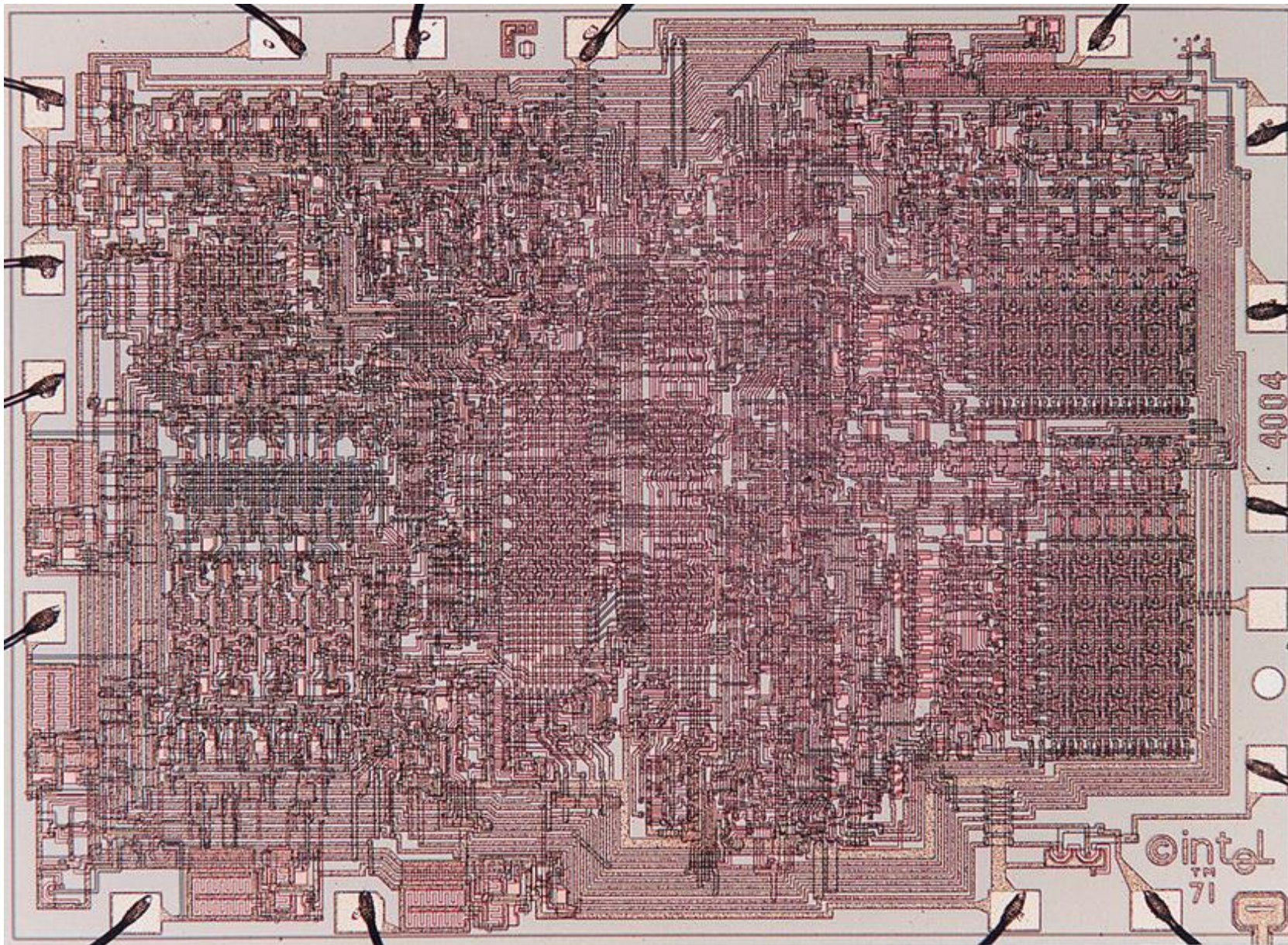
02

Tehnologija ASIC/FPGA, načrtovalski cikel

*ASIC/FPGA technology,
design flow*

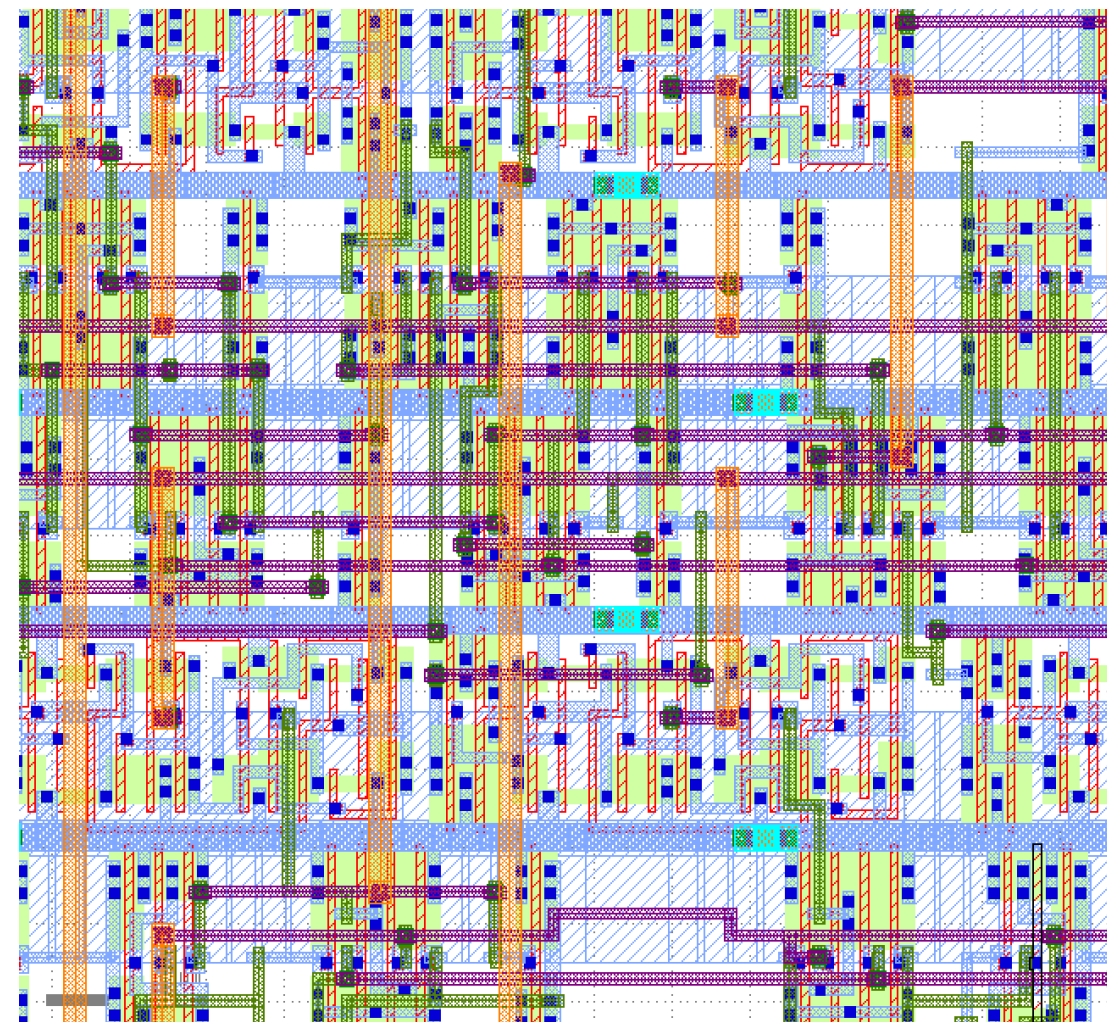
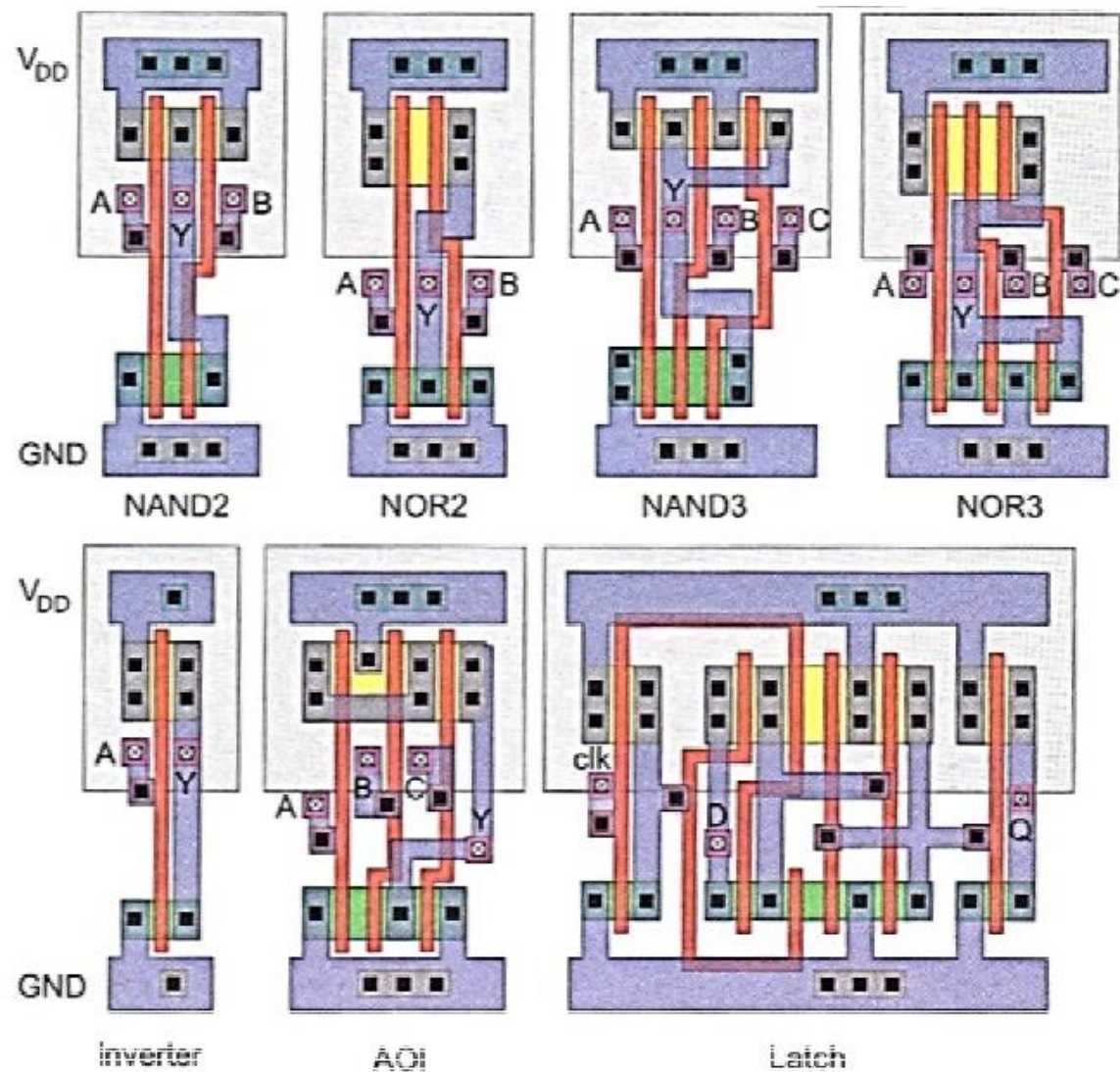
Digitalno načrtovanje *Digital design*

Patricio Bulić in Nejc Ilc

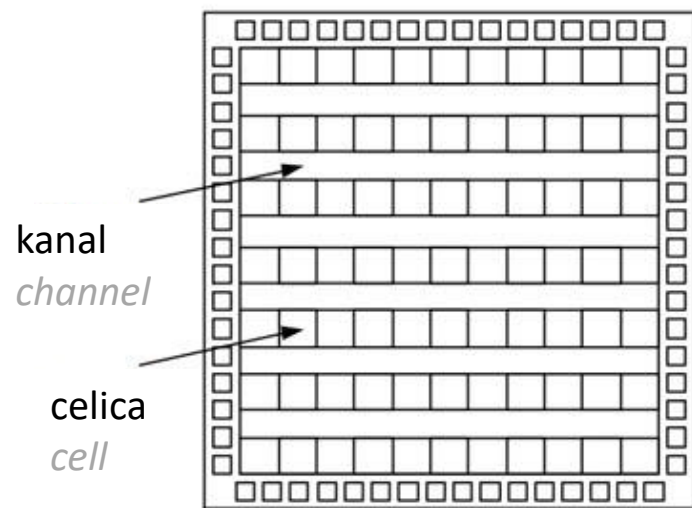


ASIC – popolnoma po meri: Intel 4004 (1971)

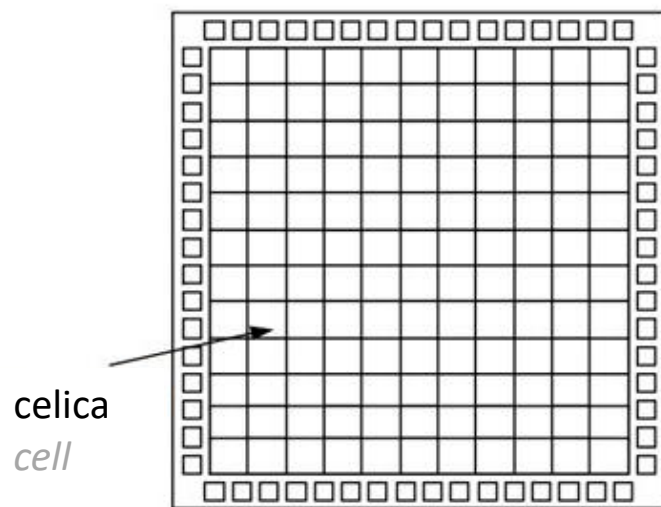
Full custom ASIC



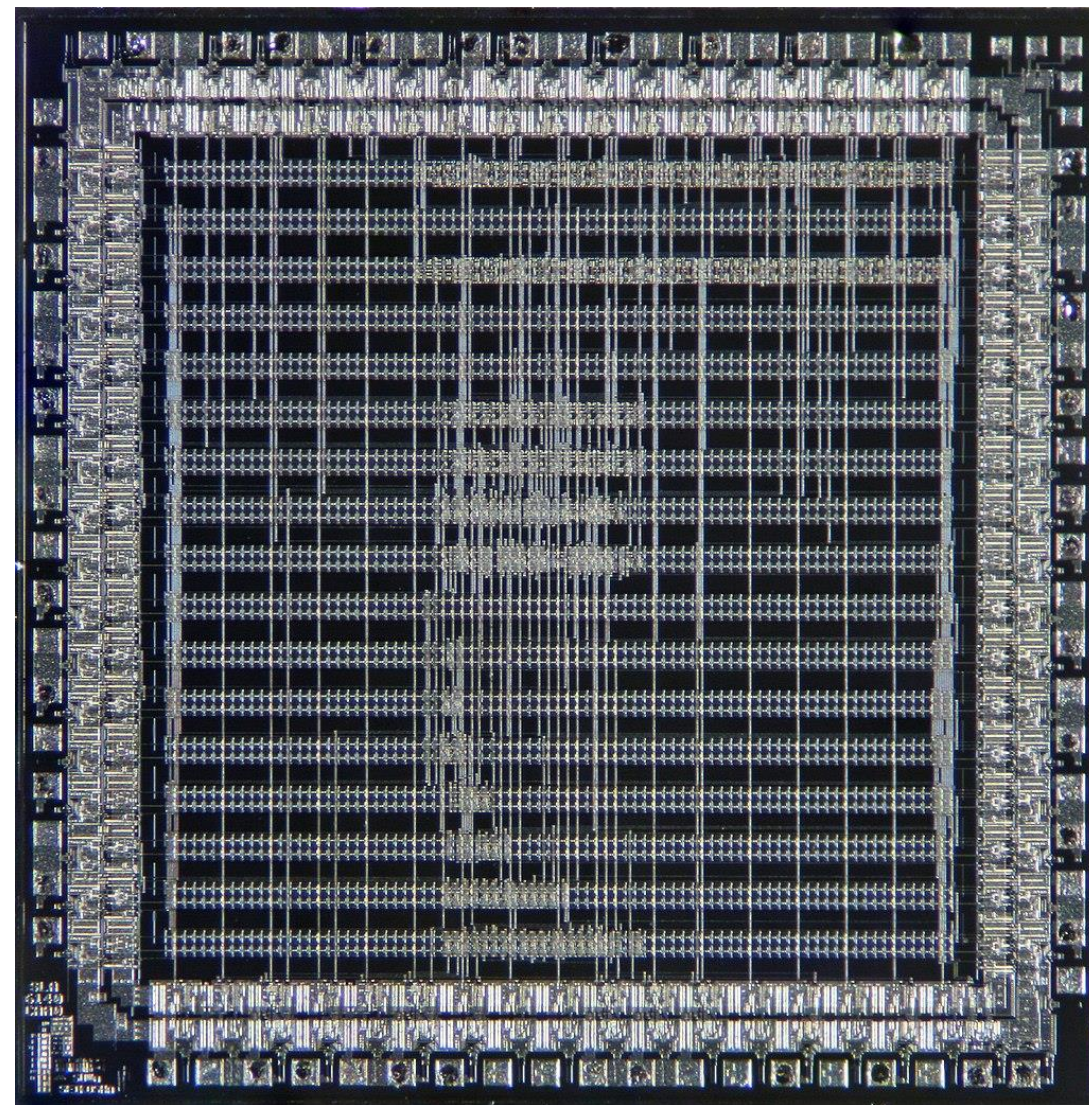
ASIC – delno po meri: CBIC (cell-based integrated circuit)
Semi-custom ASIC



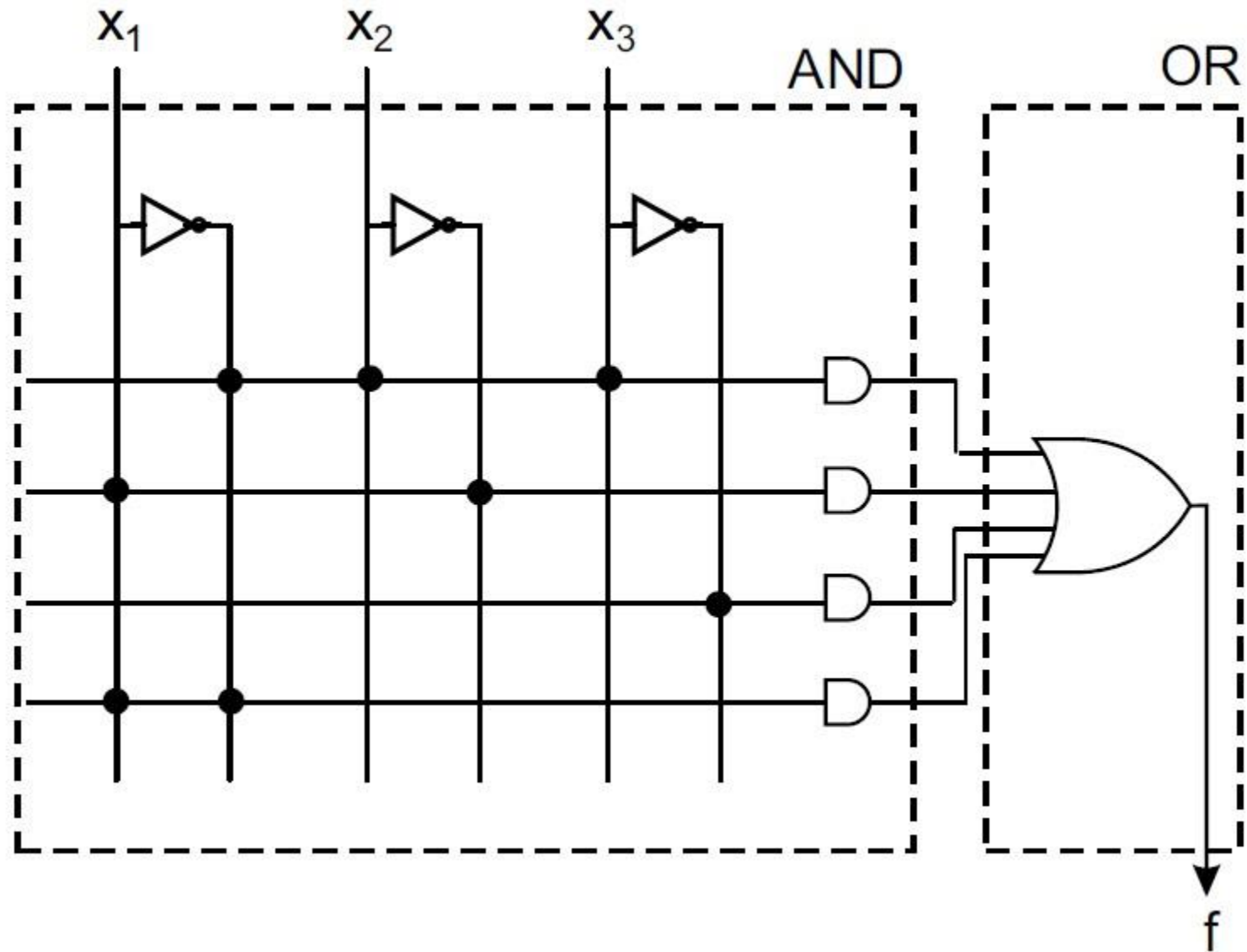
polje vrat s kanali
channeled gate array



polje vrat brez kanalov
channel-less gate array

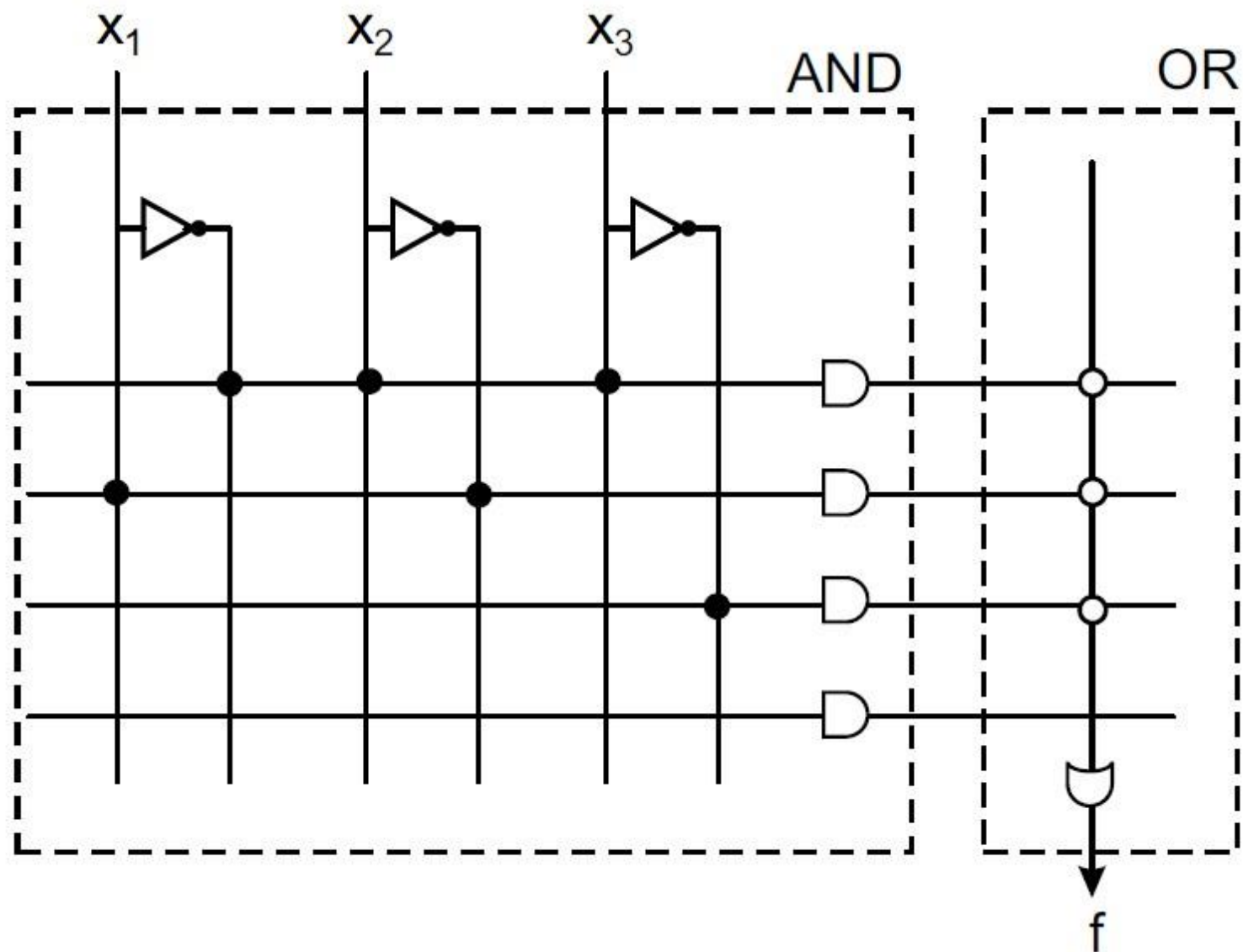


ASIC – delno po meri: polje vrat
Semi-custom ASIC: gate array



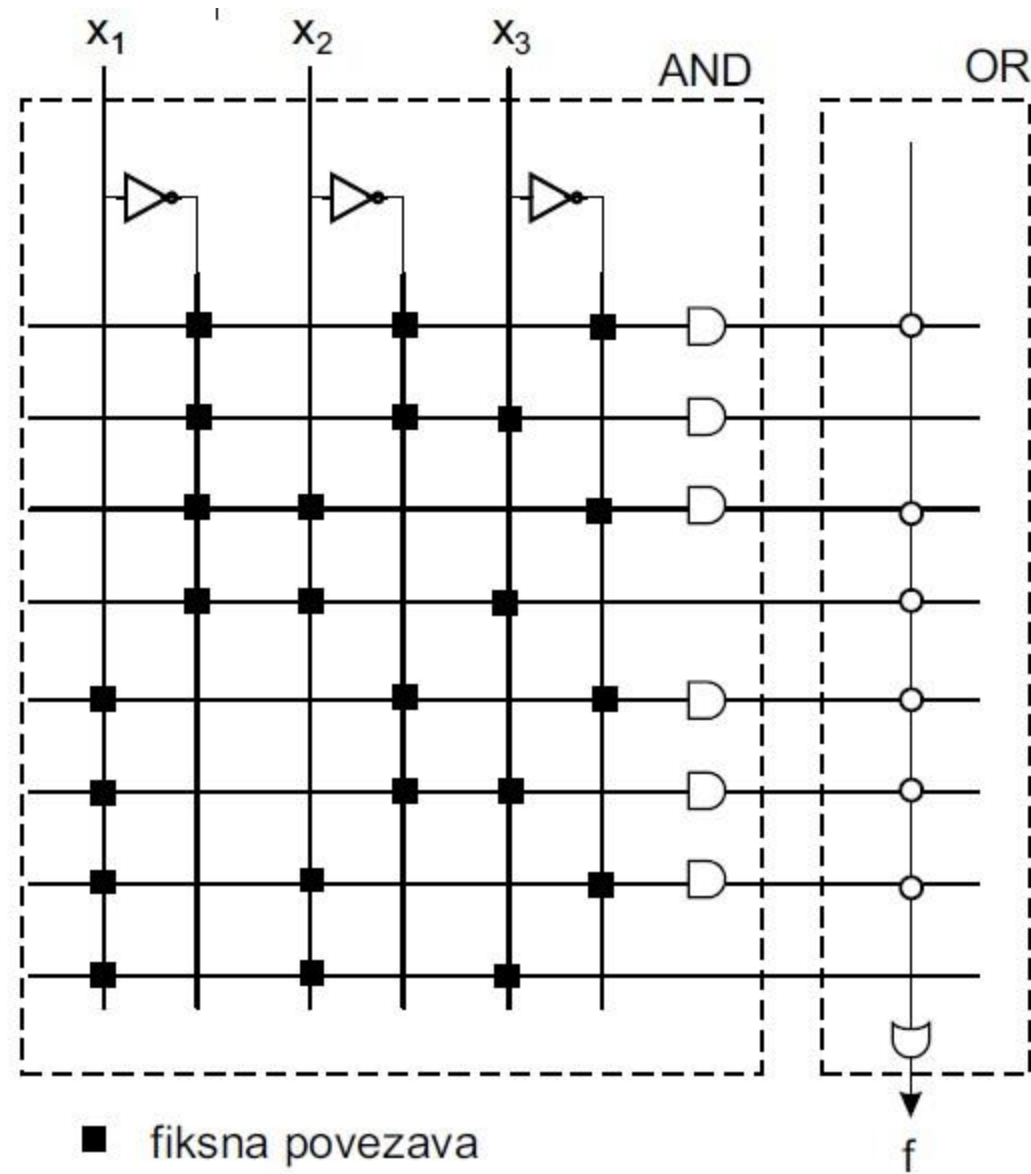
Programirljiv ASIC: PLD (programmable logic device) $\rightarrow$ PAL (programmable array logic)

Programmable ASIC: PLD $\rightarrow$ PAL



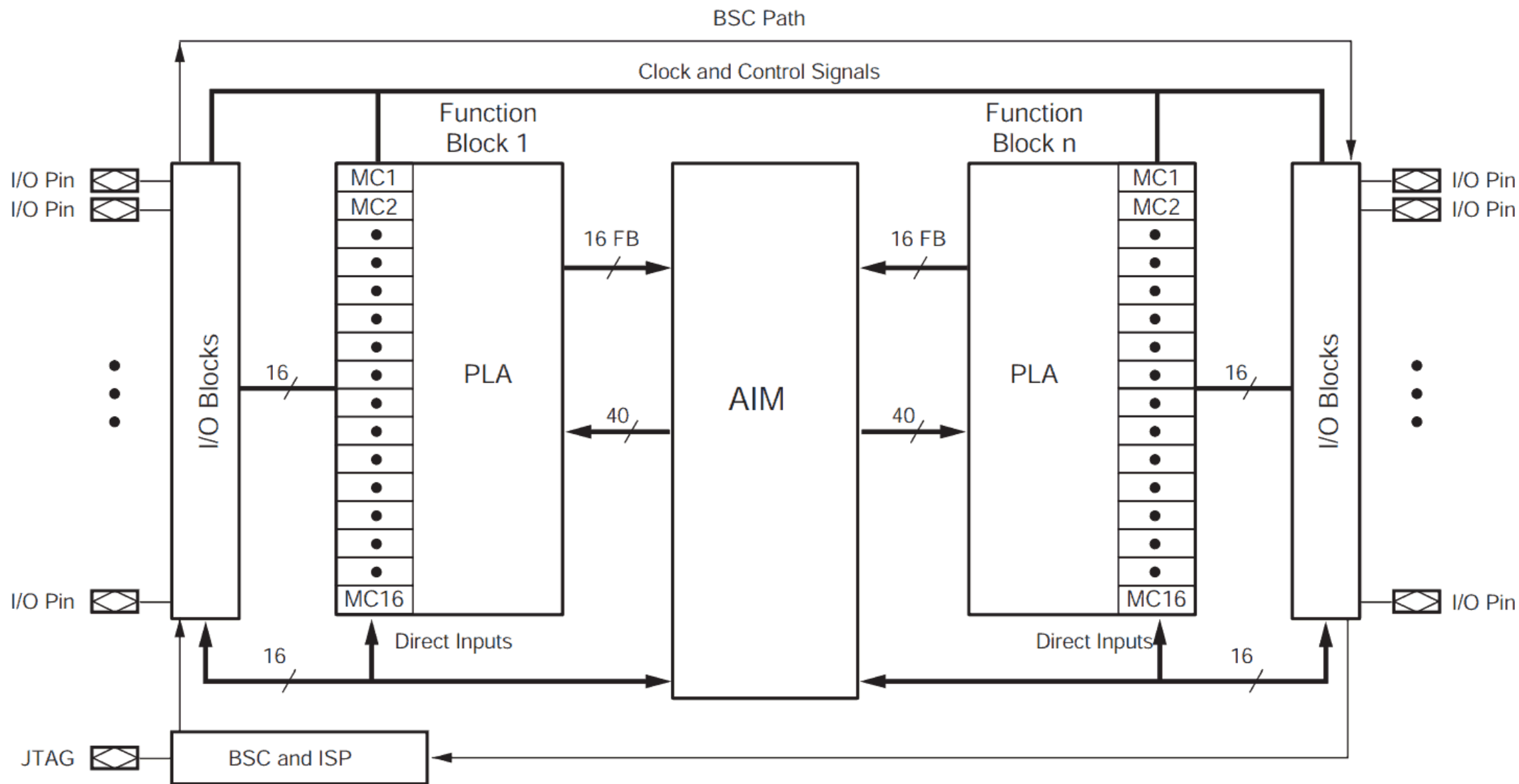
Programirljiv ASIC: PLD $\rightarrow$ PLA (programmable logic array)

Programmable ASIC: PLD $\rightarrow$ PLA



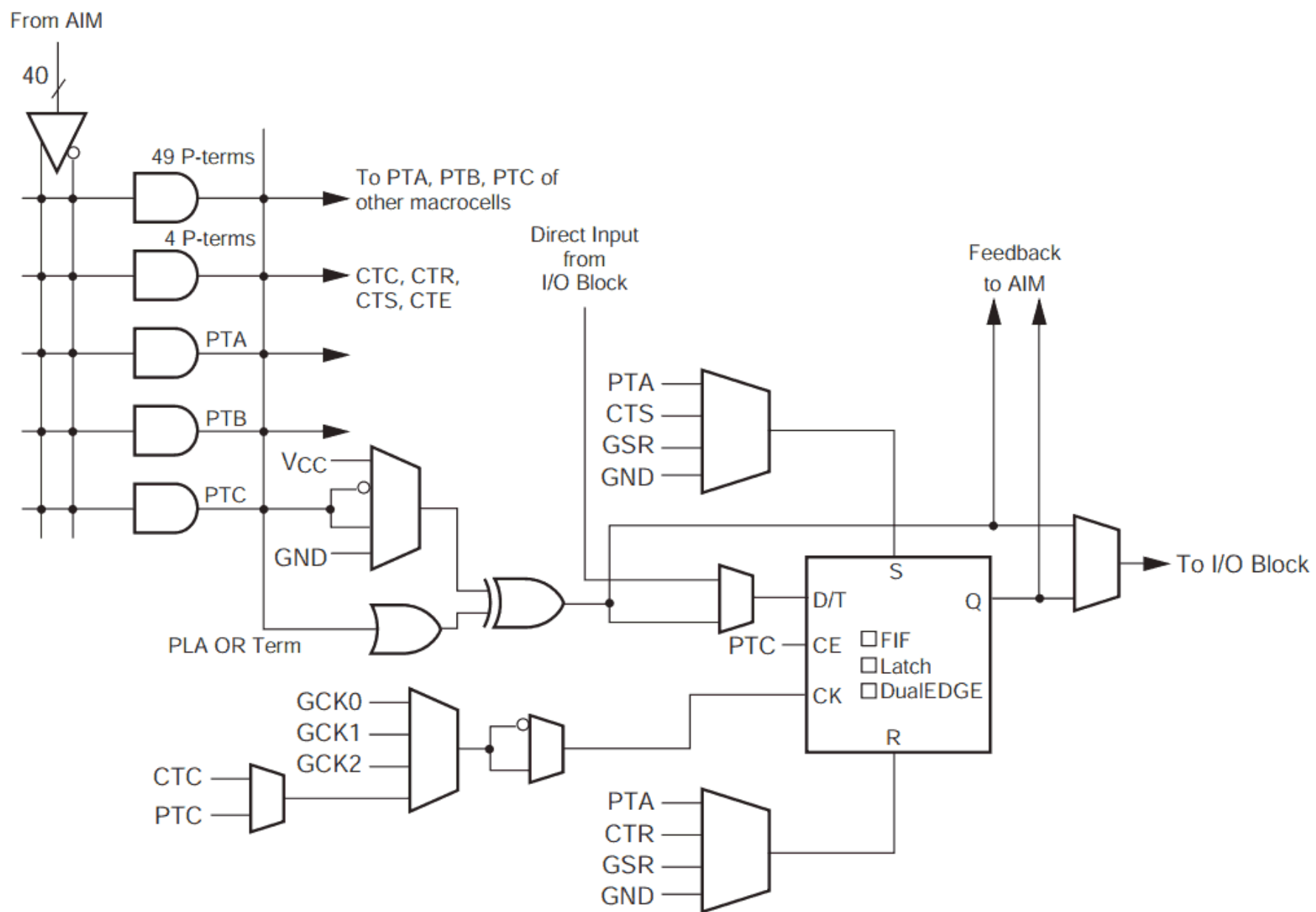
Programirljiv ASIC: PLD $\rightarrow$ PLE (programmable logic element)

Programmable ASIC: PLD $\rightarrow$ PLE

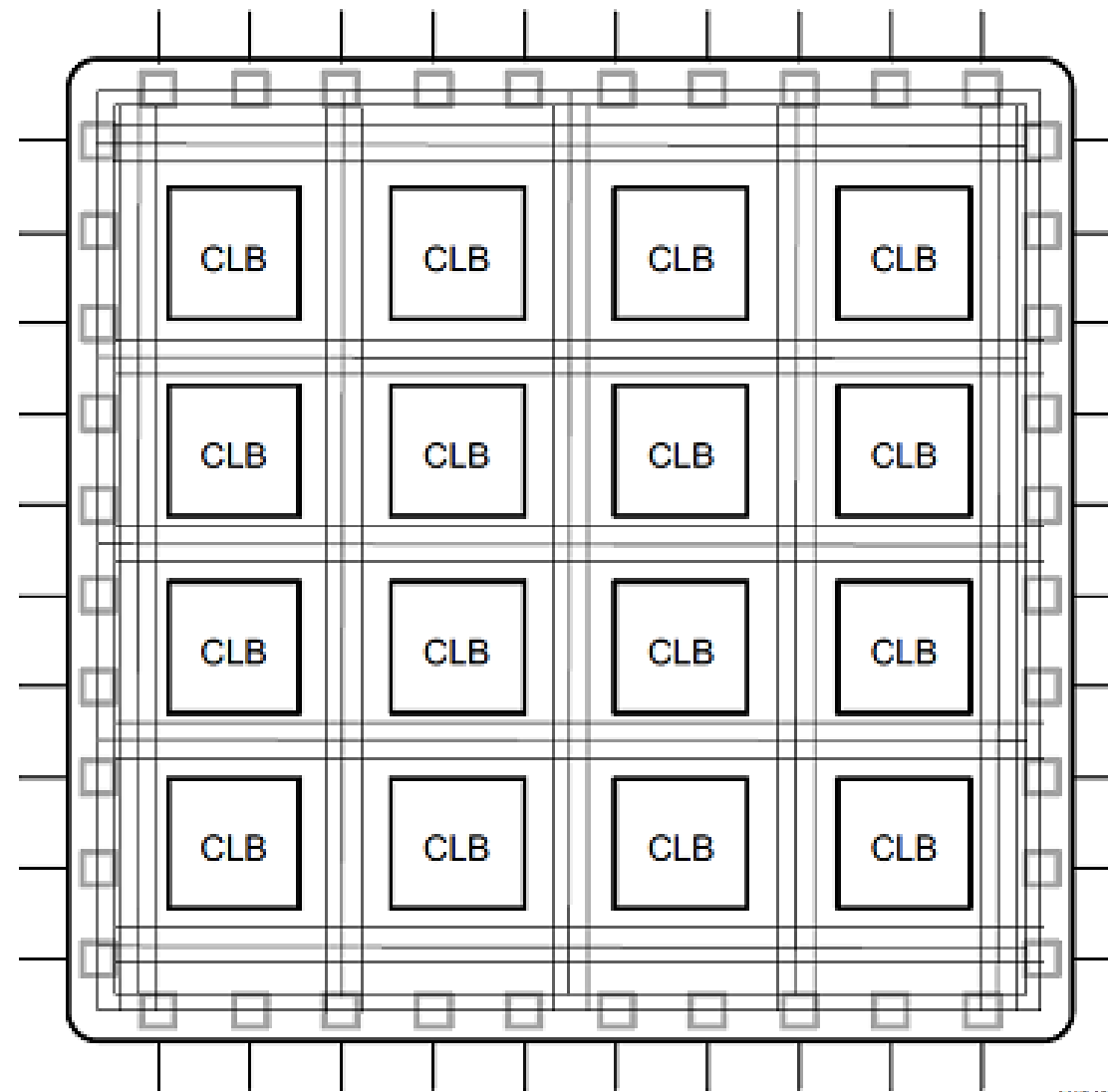


Programirljiv ASIC: CPLD (complex PLD), primer Xilinx CoolRunner II

Programmable ASIC: CPLD



Xilinx CoolRunner II: makrocelica
Macrocell

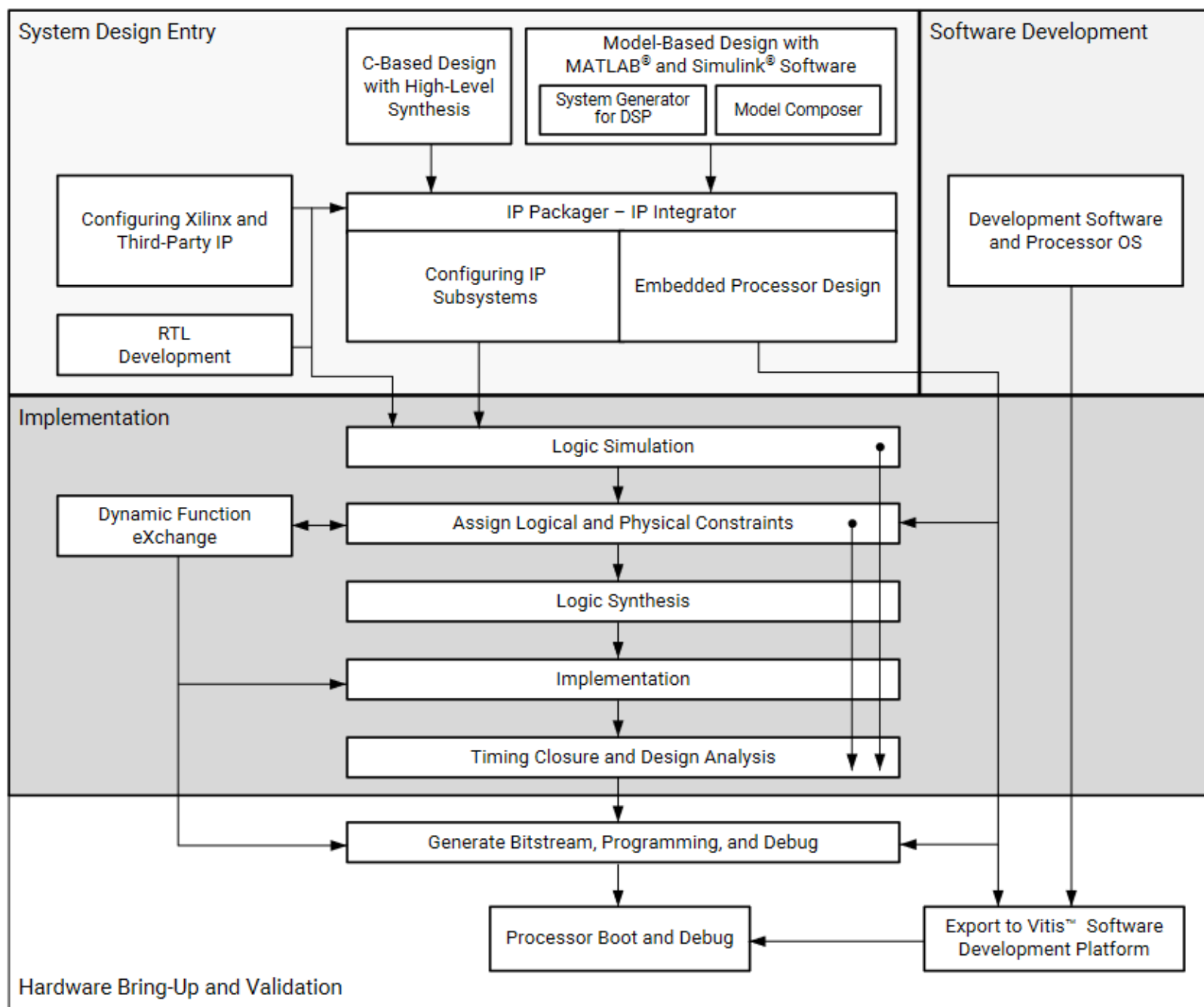


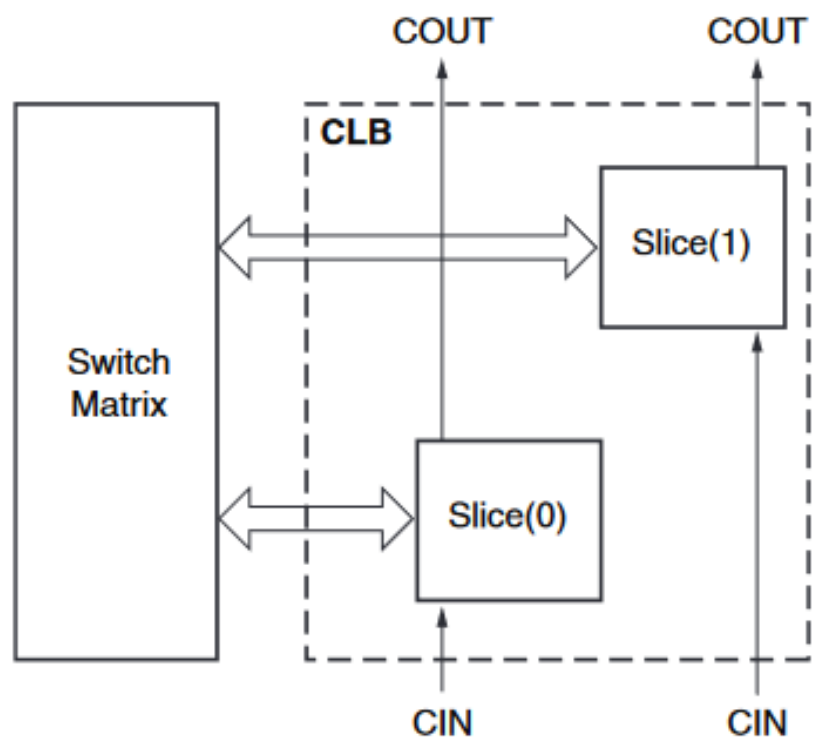
X13468

Programirljiv ASIC: FPGA (field programmable gate array) – polje programirljivih vrat

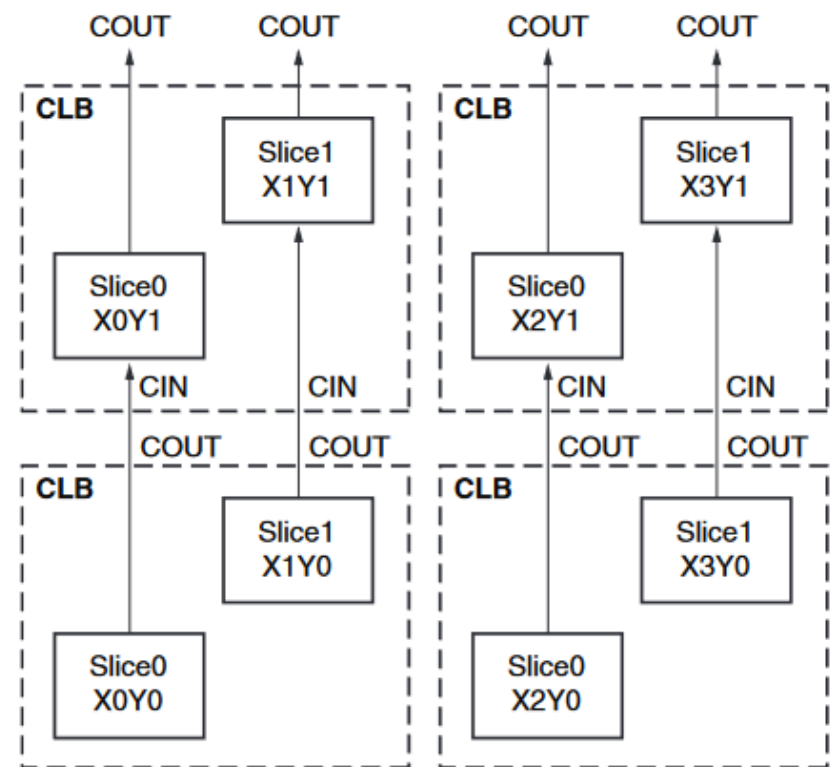
Programmable ASIC: FPGA

Figure 1: Vivado Design Suite High-Level Design Flow





UG474_c1_01_071910



UG474_c2_01_092210

Table 1-2: Artix-7 FPGA CLB Resources

Device	Slices ⁽¹⁾	SLICEL	SLICEM	6-input LUTs	Distributed RAM (Kb)	Shift Register (Kb)	Flip-Flops
7A12T	2,000 ⁽²⁾	1,316	684	8,000	171	86	16,000
7A15T	2,600 ⁽²⁾	1,800	800	10,400	200	100	20,800
7A25T	3,650	2,400	1,250	14,600	313	156	29,200
7A35T	5,200 ⁽²⁾	3,600	1,600	20,800	400	200	41,600
7A50T	8,150	5,750	2,400	32,600	600	300	65,200
7A75T	11,800 ⁽²⁾	8,232	3,568	47,200	892	446	94,400
7A100T	15,850	11,100	4,750	63,400	1,188	594	126,800
7A200T	33,650	22,100	11,550	134,600	2,888	1,444	269,200

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only SLICEMs can use their LUTs as distributed RAM or SRLs.
2. Number of slices corresponding to the number of LUTs and flip-flops supported in the device.

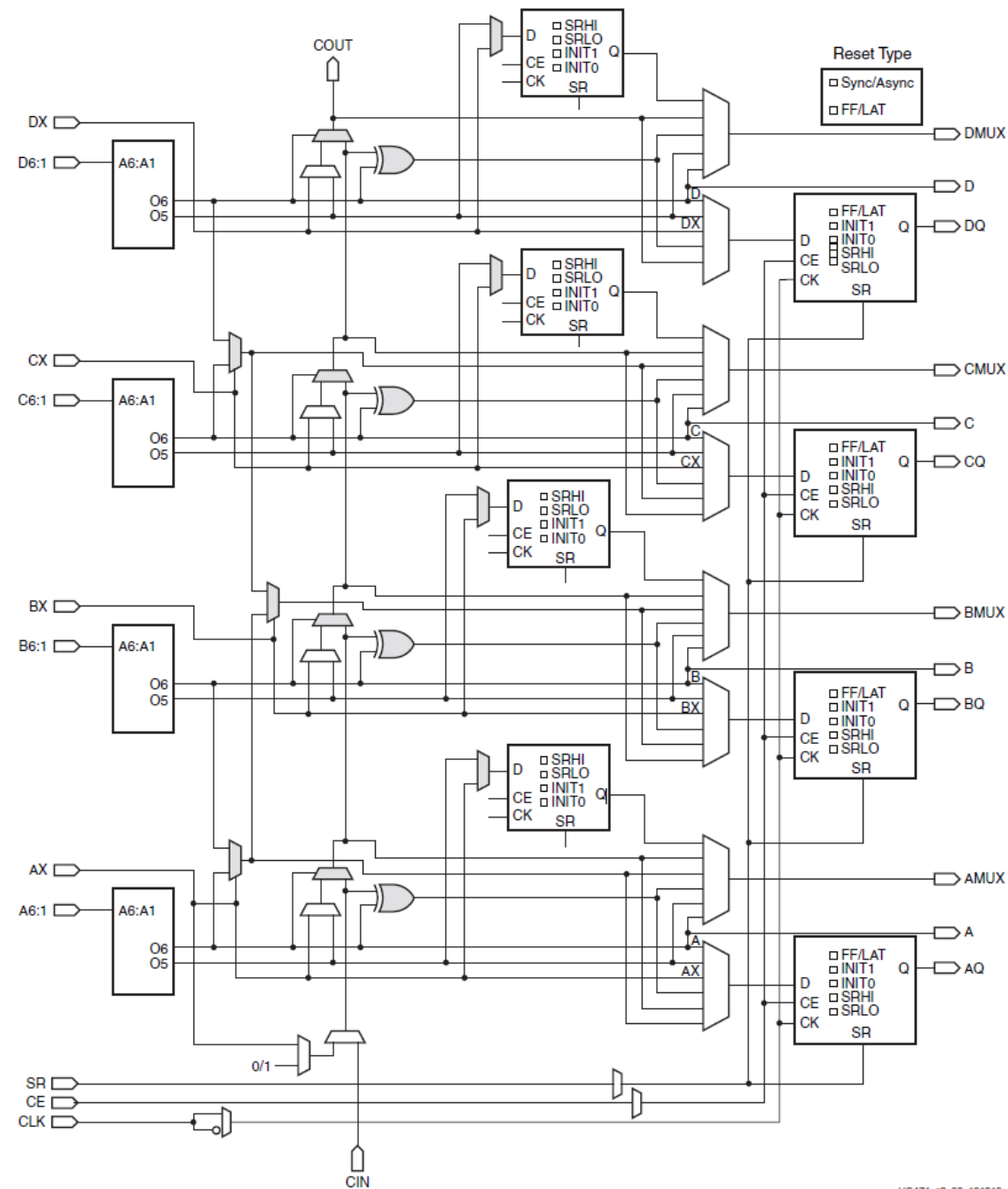


Figure 2-4: Diagram of SLICEL